7.3 Structure and role of the processor part 1

Name: _____

Class: _____

Date: _____

Time: **276 minutes**

Marks: **246 marks**

Comments:

Q1.

Employees at a bank use client computers to access data that is stored on a database server.

The database server uses software to query and modify data stored in a database on hard disk drives. It returns the results of these queries to the clients over the bank's computer network.

The performance of the system is unsatisfactory: the time-delay between a client sending a query to the server and the client receiving the results is unacceptably long.

Explain how the performance of the system might be improved. You should consider the following factors that might be affecting the performance:

- the hardware of the server
- the design of the computer network
- the database and software running on the server.

In your answer you will be assessed on your ability to follow a line of reasoning to produce a coherent, relevant and structured response.

(Total 12 marks)

Q2.

The table below shows the standard AQA assembly language instruction set. This should be used to answer question parts **(a)** and **(b)**.

`LDR Rd, <memory ref>`	Load the value stored in the memory location specified by `<memory ref>` into register `d`.
`STR Rd, <memory ref>`	Store the value that is in register `d` into the memory location specified by `<memory ref>`.
`ADD Rd, Rn, <operand2>`	Add the value specified in `<operand2>` to the value in register `n` and store the result in register `d`.
`SUB Rd, Rn, <operand2>`	Subtract the value specified by `<operand2>` from the value in register `n` and store the result in register `d`.
`MOV Rd, <operand2>`	Copy the value specified by `<operand2>` into register `d`.
`CMP Rn, <operand2>`	Compare the value stored in register `n` with the value specified by `<operand2>`.
`B <label>`	Always branch to the instruction at position `<label>` in the program.
`B<condition> <label>`	Branch to the instruction at position `<label>` if the last comparison met the criterion specified by `<condition>`. Possible values for `<condition>` and their

	meanings are: EQ: equal to NE: not equal to GT: greater than LT: less than
AND Rd, Rn, <operand2>	Perform a bitwise logical AND operation between the value in register n and the value specified by <operand2> and store the result in register d.
ORR Rd, Rn, <operand2>	Perform a bitwise logical OR operation between the value in register n and the value specified by <operand2> and store the result in register d.
EOR Rd, Rn, <operand2>	Perform a bitwise logical XOR (exclusive or) operation between the value in register n and the value specified by <operand2> and store the result in register d.
MVN Rd, <operand2>	Perform a bitwise logical NOT operation on the value specified by <operand2> and store the result in register d.
LSL Rd, Rn, <operand2>	Logically shift left the value stored in register n by the number of bits specified by <operand2> and store the result in register d.
LSR Rd, Rn, <operand2>	Logically shift right the value stored in register n by the number of bits specified by <operand2> and store the result in register d.
HALT	Stops the execution of the program.

Labels: A label is placed in the code by writing an identifier followed by a colon (:). To refer to a label the identifier of the label is placed after the branch instruction.

Interpretation of <operand2>

<operand2> can be interpreted in two different ways, depending on whether the first character is a # or an R:

- # – use the decimal value specified after the #, eg #25 means use the decimal value 25.
- Rm – use the value stored in register m, eg R6 means use the value stored in register 6.

The available general purpose registers that the programmer can use are numbered 0 to 12.

(a) **Figure 1** shows an incomplete assembly language program. The intended purpose of the code is to count from 1 to 10 inclusive, writing the values to memory location 17, which is used to control a motor.

Complete the code in **Figure 1**. You may not need to use all four lines for your solution and you should not write more than one instruction per line.

Figure 1

```
                MOV R0, #1
startloop:
                STR R0, 17
                _____________________________
                _____________________________
                _____________________________
                _____________________________
endloop:
                HALT
```

(4)

(b) `R1` contains the decimal value 7. What value will be contained in `R1` after the instruction below is executed?

```
LSL R1, R1, #2
```

_____

(1)

(Total 5 marks)

Q3.

Explain the difference between direct addressing and immediate addressing.

_____

_____

_____

_____

(Total 1 mark)

Q4.

The following registers, listed in no particular order, are used in the Fetch-Execute cycle:

- Current Instruction Register (CIR)
- Memory Address Register (MAR)
- Memory Buffer Register (MBR)
- Program Counter (PC)
- Status Register (SR)

Describe, **using full sentences**, the steps involved in the Fetch-Execute cycle.

Your description should cover the fetch, decode and execute stages of the cycle and should include an explanation of how the registers listed above are used.

You may use the abbreviations given above for the register names in your response, for example PC for Program Counter.

In your answer you will be assessed on your ability to use good English and to organise your answers clearly in complete sentences, using specialist vocabulary where appropriate.

(Total 8 marks)

Q5.

(a) Explain the effect of increasing the width of the data bus.

_____

_____

(1)

(b) Explain precisely the effect of increasing the width of the address bus by 1 bit.

_____

_____

(1)

(Total 2 marks)

Q6.

(a) What is meant by the term stored-program concept?

_____

_____

_____

_____

(2)

(b) The following registers, listed in alphabetical order, are used in the Fetch-Execute cycle:

- current instruction register (CIR)
- memory address register (MAR)
- memory buffer register (MBR)
- program counter (PC)
- status register (SR).

Describe, **using full sentences**, the steps involved in the Fetch-Execute cycle, and how the registers listed above are used. Your description should cover the fetch, decode and execute phases of the cycle.

_____

_____

_____

_____

_____

(6)

(c) Explain the term low-level language.

(1)

(d) Using the assembly language instruction `CMP R2,R3` explain the term opcode.

(1)

Instructions that can be used in question parts (e) and (f)

`LDR Rd, <memory ref>`	Load the value stored in the memory location specified by `<memory ref>` into register `d`.
`STR Rd, <memory ref>`	Store the value that is in register `d` into the memory location specified by `<memory ref>`.
`ADD Rd, Rn, <operand2>`	Add the value specified in `<operand2>` to the value in register `n` and store the result in register `d`.
`SUB Rd, Rn, <operand2>`	Subtract the value specified by `<operand2>` from the value in register `n` and store the result in register `d`.
`MOV Rd, <operand2>`	Copy the value specified by `<operand2>` into register `d`.
`CMP Rn, <operand2>`	Compare the value stored in register `n` with the value specified by `<operand2>`.
`B <label>`	Always branch to the instruction at position `<label>` in the program.
`B<condition> <label>`	Conditionally branch to the instruction at position `<label>` in

	the program if the last comparison met the criteria specified by the <condition>. Possible values for <condition> and their meaning are: • EQ: Equal to. • NE: Not equal to. • GT: Greater than. • LT: Less than.
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- # - Use the decimal value specified after the #, eg #25 means use the decimal value 25.
- Rm - Use the value stored in register m, eg R6 means use the value stored in register 6.

The available general purpose registers that the programmer can use are numbered 0 to 12.

(e) Explain what immediate addressing is **and** write an example of the use of the MOV assembly language instruction, from the table above, that uses immediate addressing.

_____

_____

_____

(2)

(f) Below is a block of program code, written in a high-level language.

```
IF X = 5
  THEN B ← 10
END IF
```

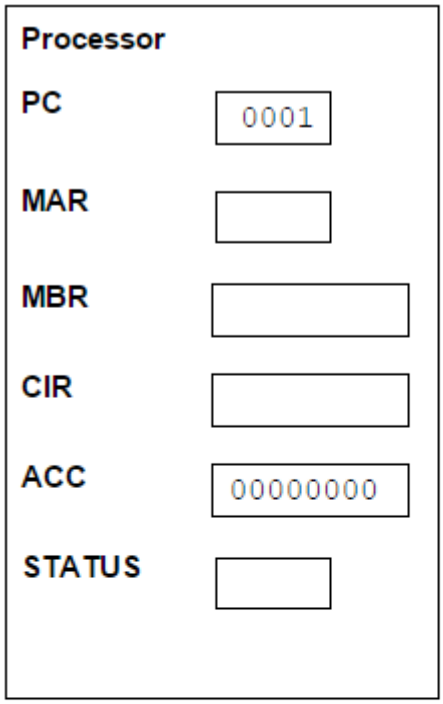
Write a sequence of assembly-language instructions that would perform the same operations as the program code above. Assume that register `R1` currently stores the value associated with `X`, register `R2` stores the value currently associated with `B` and that register `R3` is available for general use, if necessary.

(4)

(Total 16 marks)

Q7.

The diagram below shows some of the registers used in the fetch-execute cycle of a simple processor and the contents of a small section of main memory that it is connected to by the system bus (↔).



Memory Address (in binary)	Main Memory Contents (in binary)
0000	00010101
0001	00100100
0010	01000011
0011	00000000
0100	00000011
0101	00000000

OPCODE	INSTRUCTION	DESCRIPTION
0001	LOAD	Load the contents of the provided memory location into the accumulator
0010	ADD	Add the contents of the provided memory location to the current contents of the accumulator, storing the result in the accumulator
0100	STORE	Copy the contents of the accumulator into the provided memory location

(a) In the diagram above the first 4 bits of an instruction represent the opcode and give the type of instruction to be executed.

What name is given to the second 4 bits of an instruction?

_____

(1)

(b) (i) Currently the value in the Program Counter (PC) is example 0001.

Complete the table below by writing the values, expressed in binary, in the following registers after completing the fetch part of the fetch-execute cycle.

Register	Value
PC	
MAR	

MBR	

(3)

(ii) Describe what will happen during the decode and execute part of the cycle.

_____

_____

_____

_____

_____

_____

_____

(3)

(c) What would be the outcome of executing the instruction `01000011`?

_____

_____

_____

_____

(1)

(Total 8 marks)

Q8.

An integrated circuit manufacturer is looking to develop a new processor.

(a) What would be the direct consequence on potential performance of

increasing the width of the data bus? _____

_____

increasing the width of the address bus? _____

_____

increasing the clock speed? _____

_____

(3)

(b) A company has designed a new peripheral and is developing the I / O controller for it.

(i) What do we mean by the term peripheral?

_____

_____

(1)

(ii) The I / O controller is an electronic circuit consisting of three parts. One of these parts is known as the I / O port.

What is the role of the I / O port?

_____

_____

(1)

(iii) Describe another part of the I / O controller.

_____

_____

(1)

(iv) Peripheral devices are not directly connected to the processor but make use of the system bus.

Give **two** reasons why it is **not** sensible to connect peripherals directly to the processor.

Reason 1 _____

_____

Reason 2 _____

_____

(2)

(Total 8 marks)

Q9.

(a) State the full names of **two** of the special purpose registers that are used in the fetch part of the fetch-execute cycle.

Register 1 _____

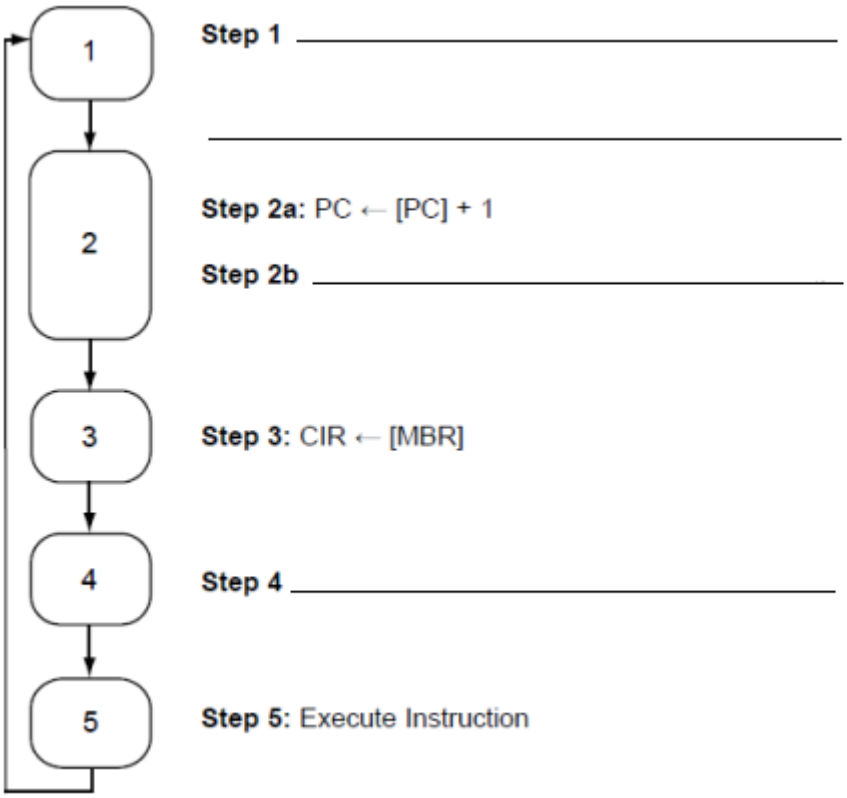
Register 2 _____

(2)

(b) **Figure 1** below is an incomplete diagram of the fetch-execute cycle.

Describe the missing steps 1, 2b and 4 using either register transfer notation or a written description. Steps 2a and 2b occur at the same time.

Figure 1



(3)

(Total 5 marks)

Q10.

A school robotics club has recently purchased a robotics kit after the teacher in charge saw an advert in a magazine. The advert is reproduced below.

RoboEddy - a new educational robot

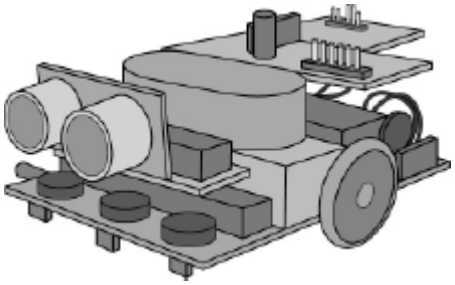
Specification

Hardware

500 Mhz processor
32 MB RAM
4 timers
Wi-Fi communications via WLAN 802.11g radio
Dual H-bridge motor driver

Software

Built in interpreter for the high level language RobotC
Directly run assembly code
XMODEM protocol for reliable file transfer
Support for various analogue and digital sensors



(a) Using the XMODEM protocol, students at the robotics club can copy a RobotC program prepared on a desktop computer to the robot.

What is meant by the term *protocol*?

_____

_____

(1)

(b) The RobotC program that has been copied to the robot can be executed by the built-in interpreter.

How does a high level language interpreter work?

_____

_____

_____

_____

(2)

(c) The robot processor is different in some ways from a processor in a desktop computer, but it still follows the stored program concept.

What is meant by the term *stored program concept*?

_____

_____

_____

_____

(3)

(d) As well as using RobotC, it is also possible to program the robot using assembly language.

The motor driver uses memory locations to store the current speed of each motor. The left motor speed is stored in memory location `21` and the right motor speed is stored in memory location `22`.

The following set of three assembly language instructions can be used to take basic

control of the motors:

`LOAD XX` - load a value from memory location XX into the accumulator

`ADD XX` - add the value stored in memory location XX to the accumulator

`STORE XX` - store the value in the accumulator in memory location XX

Selecting from the set of three instructions above, write a sequence of instructions that will swap the current left motor speed with the current right motor speed. Your program may use memory location `23` for temporary storage.

_____

_____

_____

_____

_____

_____

(3)

(e) The students develop a program that can sort coloured balls into piles but it is found that the program is not very effective.

With regards to touch and vision, state **three** factors why a robot may find a task, such as sorting coloured balls, a hard task whereas for a 4-year-old child it is a relatively easy one.

Factor 1 _____

_____

Factor 2 _____

_____

Factor 3 _____

_____

(3)

(f) The robot identifies the colour of the balls using a digital still camera component.

(i) Describe the principles of operation of a digital still camera.

_____

_____

_____

_____

_____

_____

(3)

(ii) The digital still camera component can take high resolution images but the students have chosen to program it to take low resolution images instead.

Give a reason why the students might have only used a low resolution.

_____

_____

_____

(1)

(Total 16 marks)

Q11.

The data bus, control bus and address bus are three important parts of a modern computer.

(a) In this context, explain what is meant by the term *bus*.

_____

_____

_____

(2)

(b) Fill in the gaps in the paragraph below.

The data bus can be used to transfer data and _____ between the main memory and the processor. The control bus carries control signals.

An example of a control signal is _____

_____

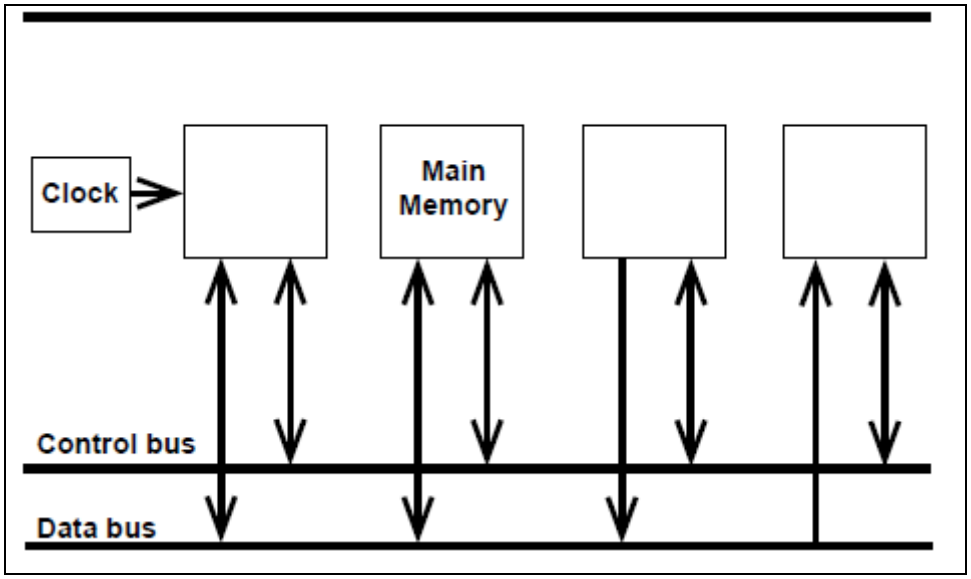
_____

(2)

(c) **Figure 1** shows some of the internal components of a computer system.

Figure 1

Address bus



On **Figure 1** label the following components.

Processor, Keyboard controller, Graphics controller

Draw **all** the connections between the address bus and the components. Make sure that you **clearly** show the direction of each connection.

(5)

(Total 9 marks)

Q12.

(a) A machine code instruction can be split into an opcode part and an operand part.

(i) What does an opcode represent?

_____

_____

(1)

(ii) What does an operand represent?

_____

_____

(1)

(b) State **two** advantages of writing a program in assembly language over writing a program in machine code.

Advantage 1: _____

_____

Advantage 2: _____

_____

(2)

(Total 4 marks)

Q13.

The following registers are used in the Fetch-Execute cycle:

- Current Instruction Register (CIR)
- Memory Address Register (MAR)
- Memory Buffer Register (MBR)
- Program Counter (PC)
- Status Register (SR)

Describe, **using full sentences**, the steps involved in the Fetch-Execute cycle, making reference to how the registers above are used. Your description should cover the fetch, decode and execute phases of the cycle. You may use the abbreviations given above for the register names in your response; for example PC for Program Counter.

In your answer you will be assessed on your ability to use good English and to organise your answer clearly in complete sentences, using specialist vocabulary where appropriate.

(Total 6 marks)

Q14.

The diagram below shows program code developed using different generations of programming languages.

Program 1 (with comments)

```
//Calculate
FirstVar := 47;
SecondVar := FirstVar + 2;
FourthVar := ThirdVar;
```

Program 2 (with comments)

```
AB2F ; Load value 2F into accumulator
BC5D ; Store contents of accumulator at address 5D
E402 ; Add value 2 to accumulator
BCFF ; Store contents of accumulator at address FF
AC61 ; Load accumulator with contents of address 61
BC4A ; Store contents of accumulator at address 4A
```

(a) What generation of programming language was used to write **Program 1**?

_____

(1)

(b) Machine code can be represented in different numeric formats.

(i) Which numeric format is used by the machine code program in **Program 2**?

_____

(1)

(ii) State **one** reason for using this format.

_____

(1)

(iii) The machine for which **Program 2** has been written has limited addressing capability.

What are the lowest and highest memory addresses that can be addressed by this machine?

Lowest address: _____

Highest address: _____

(1)

(c) Give an example of a situation for which it would be appropriate to write a program in a low level language (ie machine code or assembly language).

_____

_____

(1)

(d) Explain the differences between a compiler and an interpreter

_____

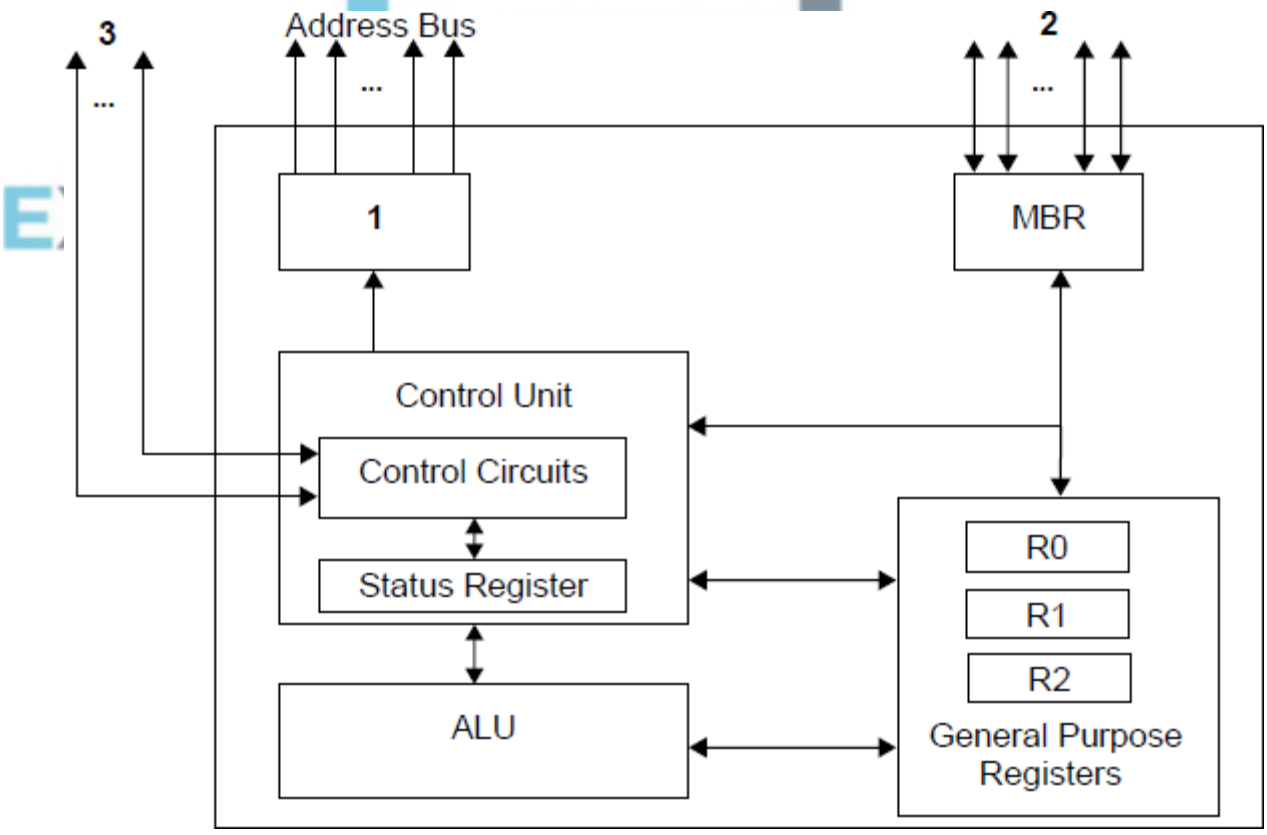
_____

(4)

(Total 9 marks)

Q15.

The diagram below shows an incomplete diagram of the components of a processor.



(a) Provide the full names for the components numbered **1** to **3** in the diagram above

by completing the table below.

Component Number	Component Name
1	
2	
3	

(3)

(b) What is the role of the Control Unit?

_____

_____

(1)

(c) State the full name of the processor component that would perform subtraction and comparison operations.

_____

_____

(1)

(d) What is meant by the term *register*?

_____

_____

(1)

(e) State **one** example of when the status register might have a bit set.

_____

_____

(1)

(Total 7 marks)

Q16.

Figure 1 and **Figure 2** show different versions of the same program.

Figure 1			Figure 2		
(x)	**(y)**	**(z)**	**(x)**	**(y)**	**(z)**
200	LOAD	7	200	01010110	00000111
201	ADD	3	201	11010000	00000011
202	ADD	6	202	11010000	00000110
203	STORE	255	203	11110000	11111111

(a) What generation of programming language is shown in **Figure 1**?

_____

(1)

(b) In both figures above there is a column labelled **(x)**.

What would be a suitable heading for this column?

_____

(1)

(c) In both tables the instruction is split into two parts.

What are the names of the instruction parts in columns **(y)** and **(z)**?

(y) _____

(z) _____

(2)

(d) What is the relationship between the instructions in **Figure 1** and **Figure 2**?

_____

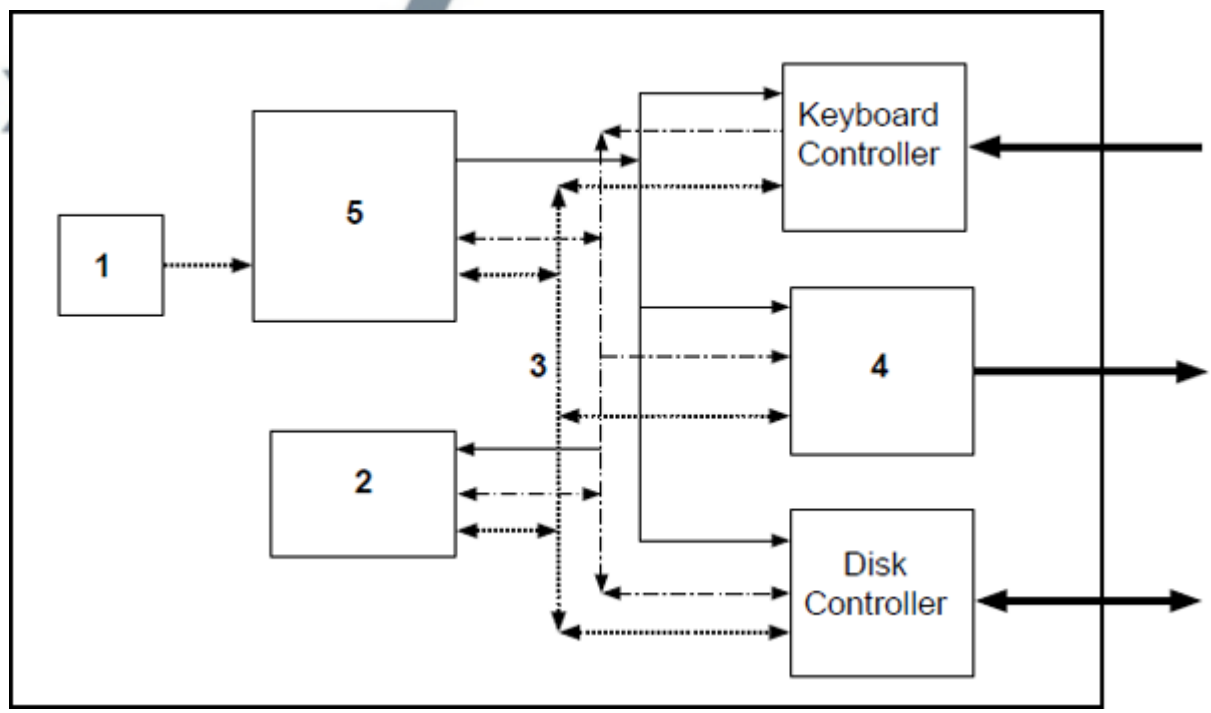
_____

(1)

(Total 5 marks)

Q17.

The diagram below shows some of the components of a computer system.



(a) Suggest names for the components numbered **1** to **5** in diagram above by

completing the table below.

Number	Component Name
1	
2	
3	
4	
5	

(5)

(b) In the first step of the Fetch-Execute Cycle the contents of the Program Counter arecopied into another register

State the **full name** of this register.

_____

(1)

(c) An item of data or an instruction fetched into the processor is initially loaded into a register.

State the **full name** of this register.

_____

(1)

(d) Modern computers often have a *64-bit address bus*.

Explain what this means.

_____

_____

(1)

(Total 8 marks)

Q18.

The internal components of a computer system are connected together by three buses.

(a) State the name of the only unidirectional bus.

_____

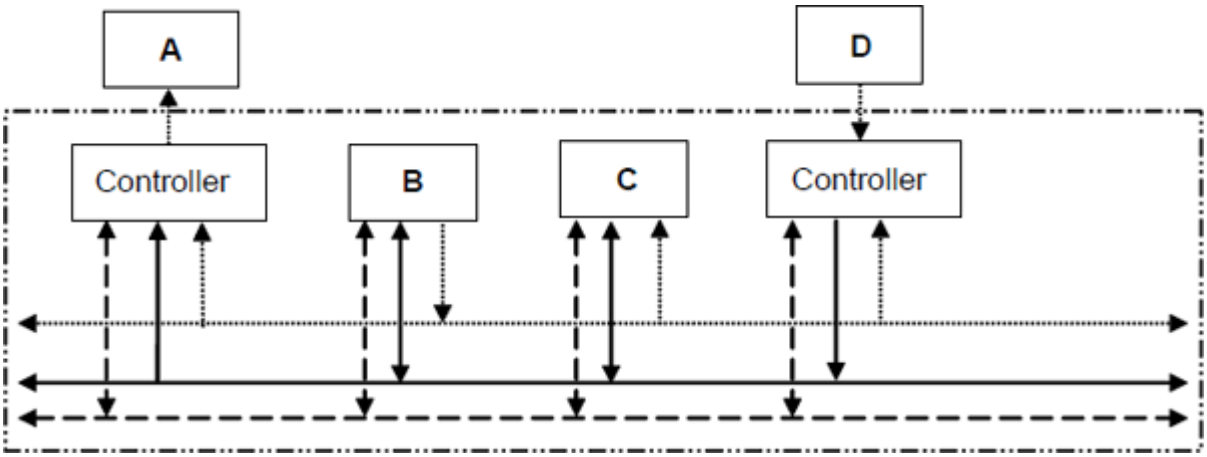
(1)

(b) If a computer has a 32-bit address bus, of 32 lines, it can access **4 gigabytes** of main memory for all forms of internal use.

How many additional lines does the address bus need for it to be capable of addressing up to **8 gigabytes** of main memory? Write your answer in the box below.

(1)

(c) The diagram below shows how components of a computer system can be connected.



Write the correct name for each of **A, B, C** and **D** from the diagram above using only the following:

Processor, Address Bus, Data Bus, Main Memory, Keyboard and Visual Display Unit

A _____

B _____

C _____

D _____

(4)

(Total 6 marks)

Q19.

Some of the assembly language instructions supported by a simple microprocessor are:

Assembly Language
STORE
LOAD
ADD

Examples of the use of these assembly language instructions are:

STORE 5	Copy the contents of the accumulator into memory location 5

`LOAD 5`	Copy the contents of memory location 5 into the accumulator
`ADD 2`	Add the contents of memory location 2 to the current contents of the accumulator, storing the result in the accumulator

(a) Write into the table below the opcode and the operand parts of the following instruction.

`LOAD 5`

Operand	
Opcode	

(1)

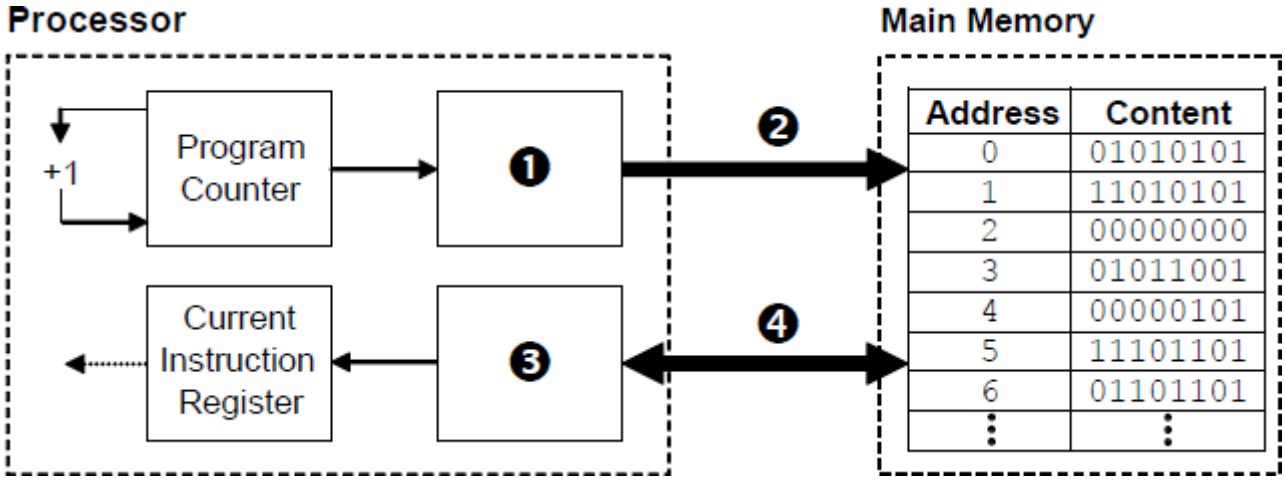
(b) Write an assembly language program, using the instructions given above, that adds the contents of memory locations 7, 8 and 3, storing the answer in memory location 21.

(3)

(Total 4 marks)

Q20.

The diagram below shows the processor registers and busses that are used during the fetch part of the fetch-execute cycle, together with the main memory. The values stored in memory locations 0 to 6 in the main memory are machine code instructions.



(a) Name the components that are labelled with the numbers 1 to 4. In the case of register names, the full names must be stated.

Number	Component Name
❶	
❷	
❸	
❹	

(4)

(b) Explain what happens during the decode and execute stages of the fetch-execute cycle.

_____

_____

_____

_____

_____

_____

(3)

(c) The machine code instructions in the main memory in the diagram above are shown in binary.
When programmers look at machine code instructions they usually prefer to view them in hexadecimal.

State **one** reason why this is the case.

_____

_____

(1)

(d) The machine code instructions in the main memory in the diagram above were produced when an assembly language program was translated into machine code.

(i) What type of program translator was used to do this?

_____

(1)

(ii) Most computer programs are initially written in an imperative high level language rather than assembly language.

Explain why this is the case.

_____

_____

_____

_____

_____

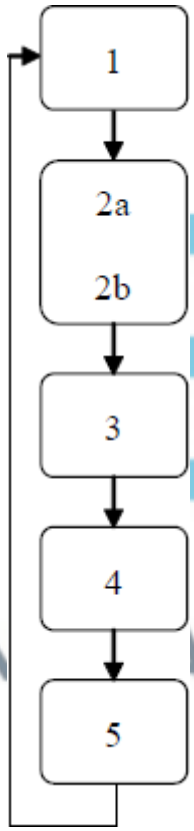
_____

(3)

(Total 12 marks)

Q21.

The figure below shows the fetch-execute cycle. Steps 2a and 2b occur at the same time.



Step 1: MAR ← [PC]

Step 2a: PC ← [PC] + 1

Step 2b: MBR ← [Memory]$_{addressed}$

Step 3: CIR ← [MBR]

Step 4: Decode Instruction

Step 5: Execute Instruction

(a) State the full names of **two** of the special purpose registers that are used in the fetch part of the fetch-execute cycle.

Register 1: _____

Register 2: _____

(2)

(b) Explain the role of the address bus, data bus and main memory during Steps 1 and 2b.

_____

_____

_____

_____

_____

(2)

(c) Give **one** reason why Steps 2a and 2b are able to occur at the same time.

_____

_____

(1)

(Total 5 marks)

Q22.

A single accumulator microprocessor supports the assembly language instructions:

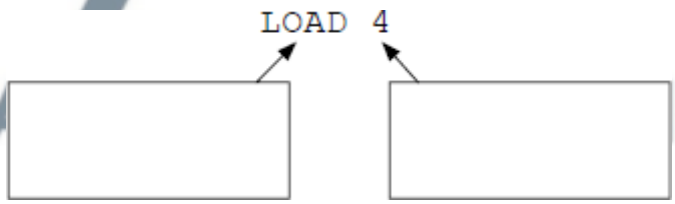
```
LOAD      memory reference
ADD       memory reference
STORE     memory reference
```

An example instruction is:

```
LOAD 4
```

which would copy the contents of the referenced memory location 4 into the accumulator register.

(a) (i) Identify which part of the instruction is the *operand* and which part is the *opcode* by writing the words operand and opcode in the two boxes below.



(1)

(ii) The accumulator is a general purpose register.

What is a *register*?

_____

_____

(1)

(b) Using the given assembly language instructions, write an assembly language program that adds together the values stored in memory locations 12 and 13, storing the resulting total in memory location 14.

_____

_____

_____

_____

_____

(3)

(Total 5 marks)

Q23.

(a) Bitmapped graphic images are composed of **pixels**.

State what is meant by a pixel.

_____

_____

_____

_____

(2)

(b) Any black and white image will require only a single bit to encode each pixel.

Figure 1 shows a black and white bitmapped image.
Figure 2 shows the memory locations where the image is stored.
The first byte used for the pixel data is at location 187.
The pixel data are stored row-by-row, starting with row 1:

- black pixels are encoded with the bit set to 1
- white pixels are encoded with the bit set to 0 .

Figure 1

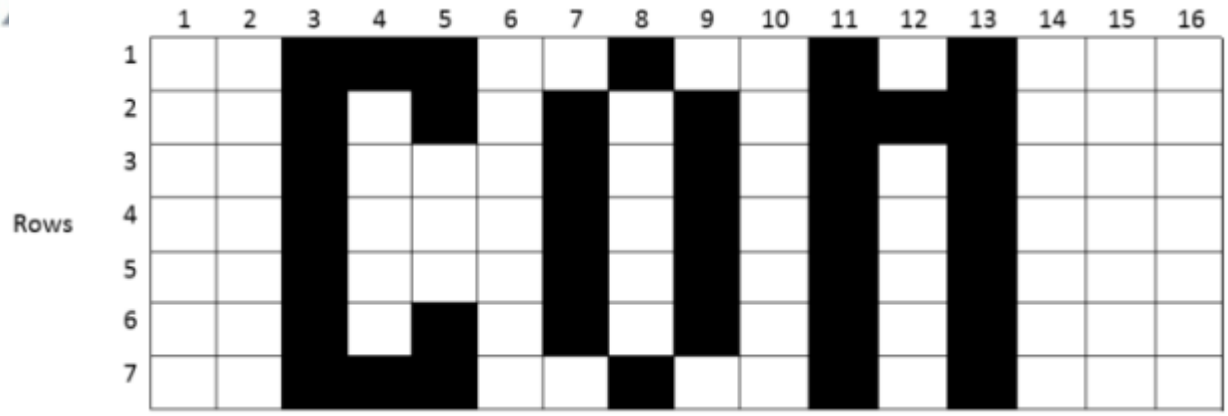


Figure 2

Location	Contents
187	0011 1001

188	0010 1000
189	
190	
:	
:	
:	
200	0010 1000

(i) What will be the contents of location 189 in **binary**?

Use the grid for rough working.

(1)

(ii) What will be the contents of location 190 in **denary**?

_____

_____

(1)

(c) Colour images can also be encoded as bitmaps.

(i) Explain how the colour of each pixel is encoded.

_____

_____

(1)

(ii) How many bits are required to store each pixel for a 256-colour image?

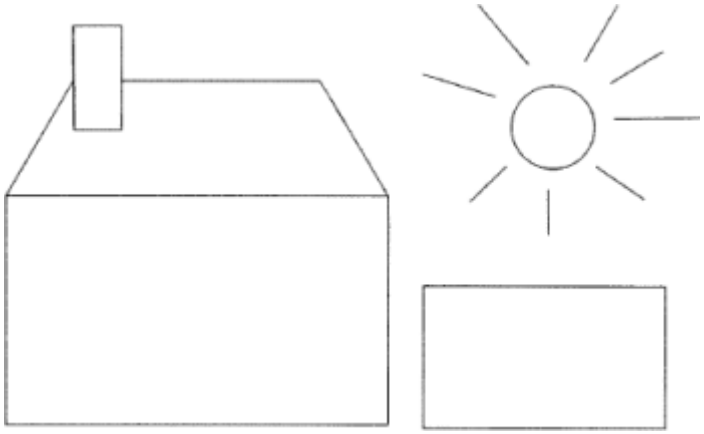
_____

_____

(1)

(d) The image in **Figure 3** was created with a vector graphics program.

Figure 3



(i) Describe how a vector graphics program stores the data about the image.

(2)

(ii) Name **three** properties that would be stored for a circle object.

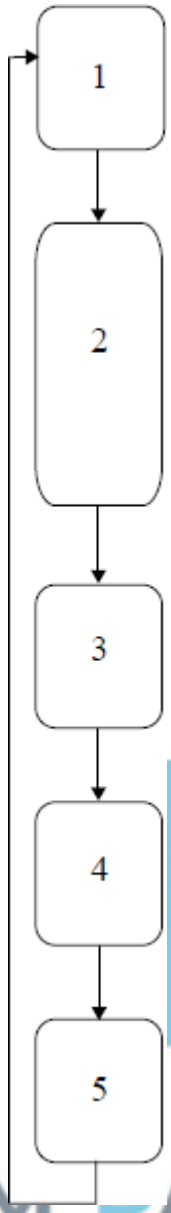
(3)

(Total 11 marks)

Q24.

The diagram below shows the fetch-execute cycle. Some of the steps have been described.

(a) Describe the missing steps 1, 2b and 4 using either register transfer notation or a written description. Steps 2a and 2b occur at the same time.



Step 1: _____

_____

Step 2a: PC ← [PC] + 1
(Increment contents of Program Counter Register)

Step 2b: _____

_____

Step 3: CIR ← [MBR]
(Transfer contents of Memory Buffer Register into Current Instruction Register)

Step 4: _____

_____

Step 5: Execute Instruction

(3)

(b) What would be the effect on the performance of the computer system of increasing the

(i) width of the data bus? _____

_____

_____

(ii) width of the address bus? _____

_____

_____

(iii) clock speed? _____

_____

_____

(3)

(Total 6 marks)

Q25.

(a) The high-level language statement

```
A := B + 5
```

is to be written in assembly language.

Complete the following assembly language statements, which are to be the equivalent of the above high level language statement. The `Load` and `Store` instructions imply the use of the accumulator register.

```
Load _________

___________ #5

Store ________
```

(3)

(b) (i) What type of translator is required to translate assembly code statements into machine code?

_____

(1)

(ii) What type of translator is required to translate a high-level language statement into machine code?

_____

(1)

(Total 5 marks)

Q26.

The Fetch-Execute cycle can be described in register-transfer language as follows:

MAR← [PC]

PC ←[PC] + 1; MBR ←$[Memory]_{addressed}$

CIR← [MBR]

[CIR] decoded and executed

where [ ] means *contents of*.

Describe the Fetch-Execute cycle in your own words.

_____

_____

_____

_____

_____

_____

_____

_____

_____

(Total 6 marks)

Q27.

Figure 1 and **Figure 2** show two different versions of a **small section of a program.**

Figure 1

```
Load    113,  R1
Load    114,  R2
Load    115,  R3
Add     R1,   R2
Add     R3,   R2
Store   R2,   160
End
```

Figure 2

(a) Main memory

100	10000000 01110001
101	10000001 01110010
102	10000010 01110011
103	11110000 00000000
104	11110011 00000000
105	00010001 10100000
106	00000000 00000000

(a) In **Figure 2** the label is missing from the column showing 100 to 106.

What should this label be? _____

(1)

(b) What generation of programming language is shown in **Figure 1**?

_____

(1)

(c) The code as written by the programmer is shown in **Figure 1**. A translator program is needed to produce a version of the code the processor can execute.

(i) What is this translator program called?

_____

(1)

(ii) Following the translation process various outputs will be produced.
One output from this translation is the machine code executable file.

Name **one** other possible output _____

(1)

(d) Many digital computers operate on the stored program concept.

Explain the *stored program concept*.

_____

_____

_____

_____

(4)

(Total 8 marks)

Q28.

A computer system has the following assembly code instructions that you are to use in this question:

Label	Opcode	Operand (s)	Description
	AND	#nn	Logical AND the accumulator with hexadecimal value nn
	OR	#nn	Logical OR the accumulator with hexadecimal value nn
	LD	nnnn	Load contents of hexadecimal address nnnn into the accumulator
	LD	label	Load contents of labelled memory into the accumulator
	ST	nnnn	Store contents of the accumulator into hexadecimal address nnnn
	ST	label	Store contents of the accumulator into labelled memory
	ADD	#nn	Add the hexadecimal value nn to the accumulator
	ADD	nnnn	Add the contents of hexadecimal address nnnn to the accumulator
	MUL	#nn	Multiply the accumulator by the hexadecimal value nn
	MUL	nnnn	Multiply the accumulator by the contents of the hexadecimal address nnnn
	CMP	#nn	Compare the accumulator with hexadecimal value nn
	CMP	label	Compare the accumulator with the contents of the labelled memory

	JP	label	Jump unconditionally to the label
	JE	label	Jump to the label if the result of a compare shows the accumulator to be equal to the operand
	JNE	label	Jump to the label if the result of a compare shows the accumulator not to be equal to the operand
	JG	label	Jump to the label if the result of a compare shows the accumulator to be greater than the operand
	JGE	label	Jump to the label if the result of a compare shows the accumulator to be greater than or equal to the operand
	JL	label	Jump to the label if the result of a compare shows the accumulator to be less than the operand
	JLE	label	Jump to the label if the result of a compare shows the accumulator to be less than or equal to the operand

(a) Give **two** reasons why some software is still developed in an assembly language.

1. _____

_____

2. _____

_____

(2)

(b) Give **one** reason why the majority of software is no longer developed using assembly language.

_____

(1)

(Total 3 marks)

Q29.

You want to improve the performance of your PC by upgrading certain components, whilst retaining the same motherboard.

What upgraded/additional components would bring about the following improvements? Your components for parts (a), (b) and (c) **must** be different.

(a) Increasing the speed at which application programs are executed.

Component: _____

Explanation: _____

_____

(2)

(b) Avoiding the need to continually archive picture and music files to CD storage.

Component: _____

Explanation: _____

_____

(2)

(c) Having several additional devices connected at the same time to your computer. For example, a digital camera and memory card reader.

Component: _____

Explanation: _____

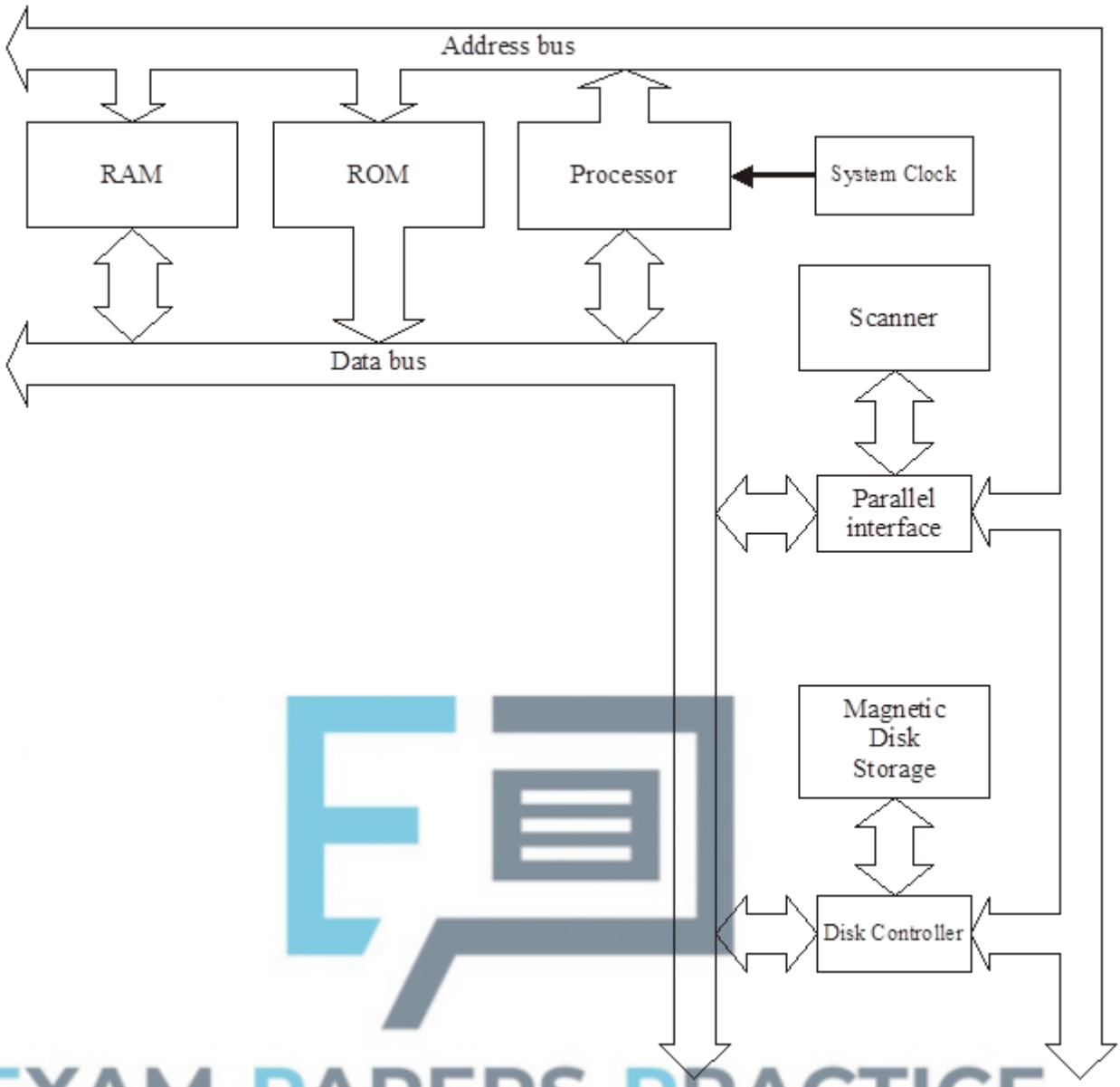
_____

(2)

(Total 6 marks)

Q30.

The figure below shows an incomplete diagram of a typical computer system architecture.



(a) Two of the components shown in the figure for a typical PC, are the RAM and the Magnetic Disk Storage. Select from the list below a typical specification value for each component.

300 GB 2 MHz 1 GB 128 kbps 3.0 MHz

(i) RAM _____

(1)

(ii) Magnetic Disk Storage _____

(1)

(b) A third bus has been omitted from the diagram in the figure above.

Name this bus. _____

(1)

(c) Explain why the data bus is bi-directional, but the address bus is one-way only.

_____

_____

_____

_____

(2)

(d) The processor performs different types of operations; for example, arithmetic operations.

Name **one** other type of operation. _____

_____

(1)

(e) Explain the **stored program concept**. _____

_____

_____

_____

(3)

(Total 9 marks)

Q31.

A processor contains an Arithmetic Logic Unit, a control unit and a number of registers.

(a) What is the function of the Arithmetic Logic Unit?

_____

_____

(1)

(b) What is the function of the control unit?

_____

_____

(1)

(c) Registers may be general purpose or special purpose. Name **three** special purpose registers (do not use abbreviations).

1. _____

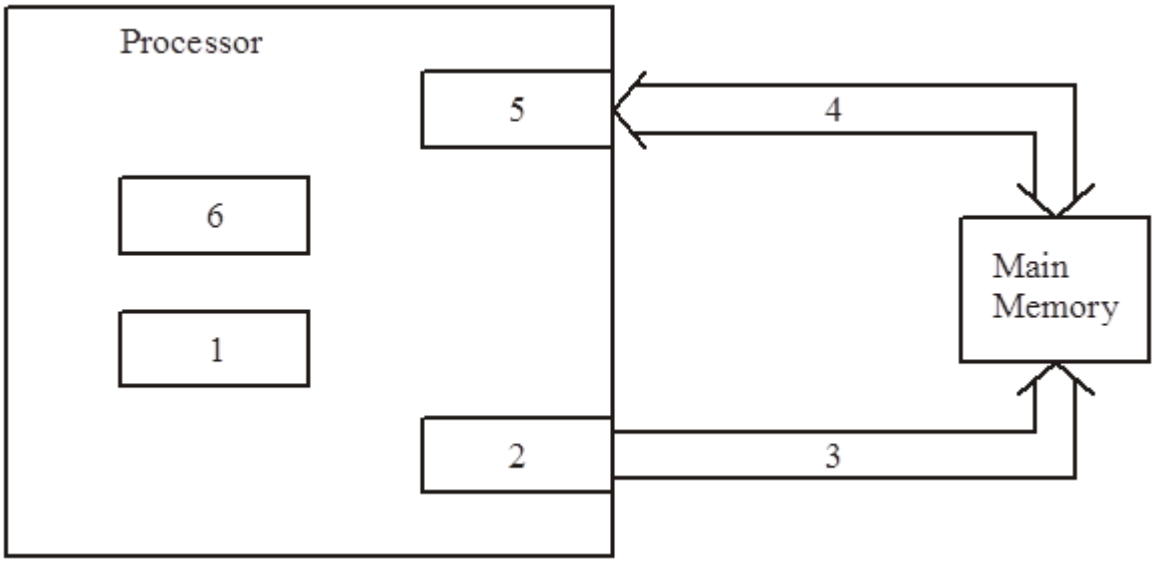
2. _____

3. _____

(3)

(Total 5 marks)

Q32.



As part of the fetch-execute cycle of a computer system the processor has to fetch the next instruction. The figure above shows the main components used. They are used in the sequence 1, 2, 3, 4, 5, 6 to fetch the next instruction. Name the components by completing the table below.

Component	Name
1	Program Counter
2	
3	
4	
5	
6	

(Total 5 marks)

Q33.

A computer system has a clock speed of 1 GHz, a 16-bit data bus and a 24-bit address bus. What would be the precise effect of

(a) increasing the clock speed to 2 GHz?

_____

_____

_____

(1)

(b) increasing the size of the data bus to 32 bits?

_____

_____

_____

(1)

(c) increasing the width of the address bus to 32 bits?

_____

_____

_____

_____

(2)

(Total 4 marks)

Q34.

Figure 1 and **Figure 2** below show **two** versions of the same program.

Figure 1

Move	#45,	R0
Move	#4,	R1
Move	#96,	R2
Add	R2,	R1
Add	R1,	R0

Figure 2

	(c)
100	00101000 00101101
101	00101001 00000100
102	00101010 01100000
103	10100001 00000000
104	10100000 00000000

(a) What generation of programming language is shown in **Figure 1**?

_____

(1)

(b) What generation of programming language is shown in **Figure 2**?

_____

(1)

(c) What would be a suitable heading for the column labelled (c) in **Figure 2**?

_____

(1)

(d) What software will be needed to translate the program code shown in **Figure 1** to the program code shown in **Figure 2**?

_____

(1)

(e) What is the relationship between the program instructions shown in **Figure 1**

program instructions in **Figure 2**?

_____

_____

_____

(1)

(f) In addition to the executable file, what output could the software referred to in part (d) produce?

_____

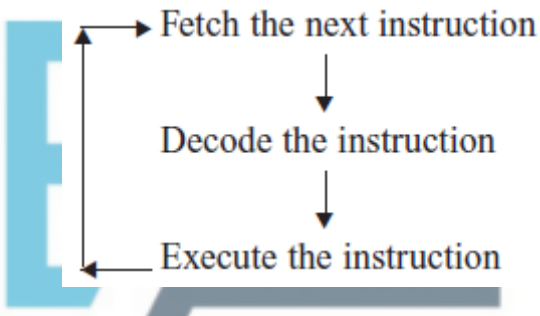
_____

(1)

(Total 6 marks)

Q35.

The fetch execute cycle may be described as:



(a) Name **four** registers that are used in the Fetch Decode part of the cycle.

1. _____

2. _____

3. _____

4. _____

(4)

(b) (i) What additional steps would be required if the computer system had an interrupt mechanism?

_____

_____

(2)

(ii) Where would they be placed in the above cycle?

_____

(1)

(c) (i) Describe the vectored interrupt mechanism.

_____

_____

_____

_____

(3)

(ii) How does this mechanism make the use of interrupts more flexible?

_____

_____

(1)

(Total 11 marks)