6.5 Boolean algebra Mark Schemes

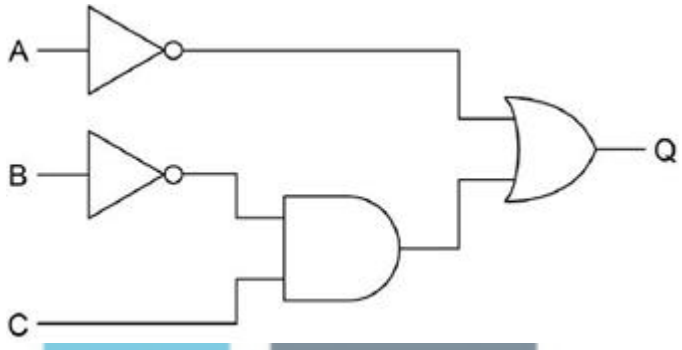
Q1.

Marks are for AO2 (apply)

1 mark for having A and B connected to (different) NOT gates;

1 mark for an AND gate connected to C and to the output of a NOT gate;

1 mark for an OR gate connected to NOT A and NOT B AND C and outputting to Q;



Max 2 if circuit not fully correct.

[3]

Q2.

Marks are for AO2 (apply)

Marking guidance for examiners

- Award marks for working out until an incorrect step has been made.
- If, in any one step, a candidate is simplifying different parts of an expression simultaneously award all relevant marks for this multiple stage but don't award any further marks for working in any parts simplified incorrectly. Example, if the expression P.P.(P+Q) + P.P.1 was changed to P.(P+Q)+P.0, the candidate would get one mark for simplifying the first part to P.(P+Q) and could get further marks for correctly simplifying this part of the expression further but should not be awarded marks for simplifying the incorrectly changed part P.0 (ie to 0)

Mark as follows

MAX 3 marks for working

Award one mark each for applying the techniques below:

- a successful application of De Morgan's Law (and any associated cancellation of NOTs) that produces a simpler expression
- successfully expanding brackets

Award one mark for each application of a Boolean identity **MAX 2**.

Note: A simpler expression is one that is logically equivalent to the original expression but uses fewer logical operators.

Example working (1)

$\overline{\overline{A \cdot \overline{B}} \cdot \overline{\overline{A} \cdot (B + B)}}$	[use of $\overline{B} + 0 = \overline{B}$]
$\overline{\overline{A \cdot \overline{B}} \cdot \overline{\overline{A} \cdot B}}$	[use of B + B = B]
$A \cdot \overline{B} + \overline{A} \cdot B$	[application of De Morgan's Law]

Example working (2)

$A \cdot (\overline{B} + 0) + \overline{A} \cdot (B + B)$	[use of De Morgan's Law]
$A \cdot \overline{B} + \overline{A} \cdot 0 + \overline{A} \cdot B + \overline{A} \cdot B$	[expansion of brackets]
$A \cdot \overline{B} + \overline{A} \cdot B + \overline{A} \cdot B$	[use of $\overline{A} \cdot 0 = 0$ and removal]
$A \cdot \overline{B} + \overline{A} \cdot B$	[application of $\overline{A} \cdot B + \overline{A} \cdot B = \overline{A} \cdot B$]

Example working (3)

$A \cdot (\overline{B} + 0) + \overline{A} \cdot (B + B)$	[use of De Morgan's Law]
$A \cdot \overline{B} + \overline{A} \cdot B$	[$\overline{B} + 0 = \overline{B}$ and B+B=B means two marks for identities within brackets]

1 mark for final answer A XOR B // A Exclusive OR B // A EOR B // A EXOR B // A ⊕ B

[4]

Q3.

All marks AO2 (apply)

Award up to four marks for the working shown, but **Max 3** if the response does not show that (A + B) · (B + C · (D + $\overline{D}$)) = A · C + B

1 mark for each application of an identity or theorem that produces an expression that is logically equivalent to the original expression but uses fewer logical operators.
1 mark for a successful application of the distribution law – only one mark, regardless of how many times this has been applied

Continue marking until an incorrect step is encountered. If a student misses out some steps but does not make an error then continue marking.

Example Solution 1

(A + B) · (B + C · (D + $\overline{D}$))	
= (A + B) · (B + C · 1)	By identity X + $\overline{X}$ = 1
= (A + B) · (B + C)	By identity X · 1 = X
= A · B + A · C + B · B + B · C	Using distribution law
= A · B + A · C + B + B · C	By identity X · X = X
= A · B + A · C + B	By redundancy theorem X + X · Y = X
= A · C + B	By redundancy theorem X + X · Y = X

Example Solution 2

(A + B) · (B + C · (D + $\overline{D}$))	
= (A + B) · (B + C · 1)	By identity X + $\overline{X}$ = 1

= (A + B) · (B + C)	By identity X · 1 = X
= A · C + B	Using distribution law (this jump is worth 2 marks)

[4]

Q4.

Marks are for AO2 (apply)

Marking guidance for examiners

- Award marks for working out until an incorrect step has been made.
- If, in any one step, a candidate is simplifying different parts of an expression simultaneously award all relevant marks for this multiple stage but don't award any further marks for working in any parts simplified incorrectly. Example, if the expression P .P .(P + Q) + P .P .1 was changed to P .(P + Q) + P .0, the candidate would get one mark for simplifying the first part to P .(P + Q) and could get further marks for correctly simplifying this part of the expression further but should not be awarded marks for simplifying the incorrectly changed part P .0 (ie to 0)

Mark as follows:

1 mark for final answer X

Max 3 marks for working:

- **1 mark** for each application of an identity other than cancelling NOTs that produces a simpler expression.
- **1 mark** for expanding brackets
- **1 mark** for putting an expression into brackets that would lead to a simpler expression.

Note: a simpler expression is one that is logically equivalent to the original expression but uses fewer logical operators.

Max 3 if answer is correct but any incorrect working or significant steps of working is missing.

Example working (1)

X. X + X. $\overline{Y}$ + Y. X + Y. $\overline{Y}$	[expansion of brackets]
X + X. $\overline{Y}$ + Y. X + 0	[use of X • X = X and Y. $\overline{Y}$ = 0]
X(1 + $\overline{Y}$ + Y) or X + X(Y + $\overline{Y}$)	[taking X outside of brackets]

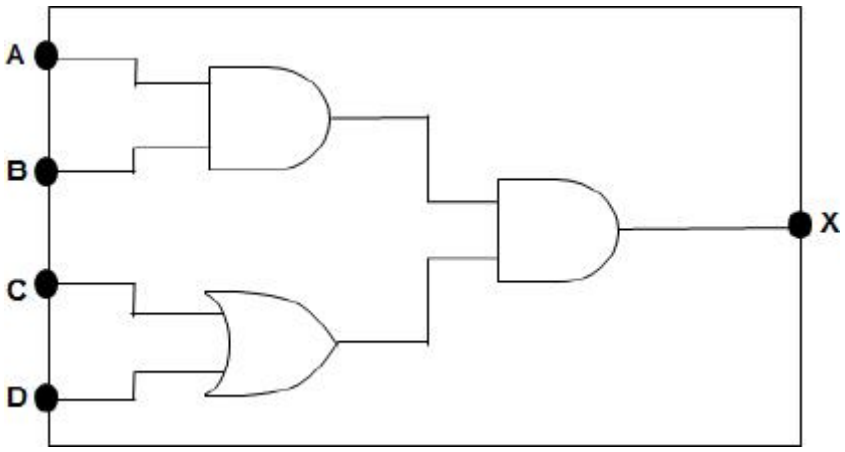
Alternative example working (2)

X + (Y. $\overline{Y}$)	[Use of distributive law]
X + 0	[Y. $\overline{Y}$ = 0]
X	[Recognising X + 0 = X]

[4]

Q5.

(a) **All marks AO2 (apply)**



1 mark: inputs A and B connected to an AND gate;
1 mark: inputs C and D connected to an OR gate;
1 mark: output of an AND gate (but not the same one as connected to inputs A and B) connected to X;

MAX 2 if circuit does not fully represent the logic of the system OR the circuit diagram contains any errors

3

(b) **All marks AO2 (apply)**

X = A • B • (C + D)
1 mark: either A • B or C + D somewhere in an incorrect expression
2 marks: fully correct expression
A. A logically equivalent expression for **2 marks**

2

[5]

Q6.

All marks AO2 (apply)

Marking guidance for examiners

- Award marks for working out until an incorrect step has been made.
- If, in any one step, a candidate is simplifying different parts of an expression simultaneously award all relevant marks for this multiple stage but don't award any further marks for working in any parts simplified incorrectly. For example, if the expression P .P .(P + Q) + P .P .1 was changed to P .(P + Q) + P .0, the candidate would get one mark for simplifying the first part to P .(P + Q) and could get further marks for correctly simplifying this part of the expression further but should not be awarded marks for simplifying the incorrectly changed part P .0 (ie to 0)

1 mark: for final answer: B + C

MAX 3 for working. Award up to two marks for applying each one of the three techniques (one mark per application):

- a successful application of De Morgan's Law (and any associated cancellation of NOTs) that produces a simpler expression.
- applying an identity other than cancelling NOTs that produces a simpler expression.
- successfully expanding brackets.

Note: A simpler expression is one that is logically equivalent to the original expression but uses fewer logical operators.

Example Working (1)

$$\overline{\left(\overline{A} + A \bullet (A + B)\right)} + (\overline{B} \bullet \overline{C})$$

$= \left(\overline{A} + A \bullet (A + B)\right) \bullet \overline{(\overline{B} \bullet \overline{C})}$ Application of DeMorgan

$= \left(\overline{A} + A \bullet (A + B)\right) \bullet (B \bullet C)$ Application of DeMorgan

$= \left(\overline{A} + A \bullet (B \bullet C)\right)$ By identity $A = A \bullet (A + B)$

$= 1 \bullet (B + C)$ By identity $\overline{A} + A = 1$

$= B + C$ By identity $1 \bullet X = X$

Example Working (2)

$$\overline{\left(\overline{A} + A \bullet (A + B)\right)} + (\overline{B} \bullet \overline{C})$$

$= \overline{\left(\overline{A} + A \bullet A + A \bullet B\right)} + (\overline{B} \bullet \overline{C})$ Expansion of brackets

$= \overline{\left(\overline{A} + A + A \bullet B\right)} + (\overline{B} \bullet \overline{C})$ By identity $A \bullet A = A$

$= \overline{(1 + A \bullet B)} + (\overline{B} \bullet \overline{C})$ By identity $\overline{A} + A = 1$

$= \overline{(1)} + (\overline{B} \bullet \overline{C})$ By identity $1 + X = 1$

$= \overline{0} + (\overline{B} \bullet \overline{C})$ By identity $\overline{0} = 1$

$= \overline{(\overline{B} \bullet \overline{C})}$ By identity $0 + X = X$

$= B + C$ Application of DeMorgan

[4]

Q7.

ALGEBRAIC SOLUTION:

$\overline{\overline{A} + \overline{B}} + B.\overline{A}$

$A.B + B.\overline{A}$ [Correct application of De Morgan's Law 1 mark]

$B.(A + \overline{A})$ [Collection of like terms 1 mark]

B [Correct answer 1 mark]

Alternative answer:

$\overline{\overline{A} + \overline{B} + B.\overline{A}}$

$\overline{(\overline{A} + \overline{B}).(B.\overline{\overline{A}})}$ [Correct application of De Morgan's Law 1 mark]

$\overline{(\overline{A} + \overline{B}).(\overline{B} + A)}$

$\overline{\overline{A}.\overline{B} + \overline{A}.A + \overline{B}.\overline{B} + \overline{B}.A}$

$\overline{\overline{A}.\overline{B} + 0 + \overline{B} + \overline{B}.A}$ $[\overline{A}.A = 0]$

$\overline{\overline{B}.(\overline{A} + 1 + A)}$ [Collection of like terms 1 mark]

$\overline{\overline{B}.(1+1)}$

$\overline{\overline{B}}$

B [Correct answer 1 mark]

A. alternative notations :

- For A · B allow A AND B, A ∧ B, A∩B, AB
- For A+B allow A OR B, A ∨ B, A∪B
- For A allow NOT A, ¬A

[3]

Q8.

Marks are for AO2 (apply)

Marking guidance for examiners

- Award marks for working out until an incorrect step has been made.
- If, in any one step, a candidate is simplifying different parts of an expression simultaneously award all relevant marks for this multiple stage but don't award any further marks for working in any parts simplified incorrectly. Example, if the expression P.P.(P + Q) + P.P.1 was changed to P.(P+Q) + P.0 the candidate would get one mark for simplifying the first part to P.(P+Q) and could get further marks for correctly simplifying this part of the expression further but should not be awarded marks for simplifying the incorrectly changed part P.0 (i.e. to 0).

Mark as follows

1 mark for final answer:

Max 3 for working; **Max 3** if answer is correct but any incorrect working or significant steps of working is missing:

1 mark for a successful application of De Morgan's Law that would lead to a simpler expression. **Max 2** for applications of De Morgan's Law.
1 mark for applying an identity other than cancelling nots that produces a simpler expression. **Max 2** for applying identities.
1 mark for expanding brackets or putting an expression into brackets that would lead to a simpler expression. **Max 2** for expanding brackets or putting an expression into brackets.

Note: a simpler expression is one that is logically equivalent to the original expression but uses fewer logical operators.

Example working (1)

$= (\overline{A} + B).(\overline{A}.(B + A))$ [application of De Morgan's law]

$= (\overline{A} + B).(\overline{A}.B + \overline{A}.A)$ [expansion of brackets]

$= (\overline{A} + B).(\overline{A}.B)$ [use of identities $X.\overline{X}$ = 0 and X+0 = X]

$= \overline{A}.\overline{A}.B + B.\overline{A}.B$ [expansion of brackets]

$= \overline{A}.B + \overline{A}.B$ [use of identity *X*.*X* = *X* twice]

$= \overline{A}.B$ [use of identity *X* + *X* = *X*]

Alternative example working (2)

$= \overline{(\overline{A} + B) + (A + (\overline{B} + A))}$ [application of De Morgan's Law]

$= \overline{A}\overline{B} + \overline{\overline{A}(B + A)}$ [application of De Morgan's Law twice]

$= \overline{A}\overline{B} + \overline{(\overline{A}.B + \overline{A}.A)}$ [expansion of brackets]

$= \overline{A}\overline{B} + \overline{\overline{A}.B}$ [use of identities $\overline{A}.A = 0$ and *X* + 0 = *X*]

$= \overline{A} + B + \overline{A}.B$ [application of De Morgan's Law]

$= (\overline{A} + B).(\overline{A}.B)$ [application of De Morgan's Law]

$= \overline{A}.\overline{A}.B + B.\overline{A}.B$ [expansion of brackets]

$= \overline{A}.B + \overline{A}.B$ [use of identity *X*.*X* = *X* twice]

$= \overline{A}.B$ [use of identity *X* + *X* = *X*]

Alternative example working (3)

$= \overline{(\overline{A} + B) + (A + (\overline{B} + A))}$ [application of De Morgan's Law]

$= \overline{A}\overline{B} + \overline{\overline{A}(B + A)}$ [De Morgan's Law twice]

$= \overline{A}\overline{B} + \overline{(\overline{A}.B + \overline{A}.A)}$ [Expansion]

$= \overline{A}\overline{B} + \overline{\overline{A}.B}$ [Identity $\overline{A}.A = 0$ and *A* + 0 = *A*]

$= \overline{A} + B + \overline{A}.B$ [application of De Morgan's Law]

$= (\overline{A} + B).(\overline{A}.B)$ [application of De Morgan's Law]

$= \overline{A}.\overline{A}.B + B.\overline{A}.B$ [Expansion]

$= \overline{A}B + \overline{A}B$ [Identity $\overline{A}.\overline{A} = \overline{A}$ and $B.B = B$]

$= \overline{A}B$ [Final answer via identity $A + A = A$]

[4]

Q9.

(a) **Mark is for AO1 (knowledge)**

XOR // EOR // Exclusive OR;

1

(b) **Mark is for AO2 (apply)**

$\overline{C}$;

1

(c) **Mark is for AO2 (apply)**

C;

1

(d) **Marks are for AO2 (apply)**

C	B	A	T	S	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0

Mark as follows:
1 mark: column T correct;
1 mark: column S correct;
1 mark: column R correct;

3

(e) **Mark is for AO2 (analyse)**

Use this circuit on the binary number to be subtracted and add the result to the other binary number;

A. Any equivalent answers
R. Number to be added IS negative

1

(f) **3 marks for AO1 (knowledge) and 3 marks for AO1 (understanding)**

1 mark for AO1 (knowledge): (increase the) data bus width;
1 mark for AO1 (understanding): enables more bits (**A.** data) to be transferred between main memory and the processor <u>at one time</u> (so fewer read/write operations needed);

1 mark for AO1 (knowledge): (increase the) clock speed;
1 mark for AO1 (understanding): enables more instructions to be executed per unit of time/second (**A.** calculations/operations/commands instead of instructions) //

each individual instruction could be executed sooner / more quickly (**A.** calculation/operation/command instead of instruction);

1 mark for AO1 (knowledge): (increase the) amount of cache memory;
1 mark for AO1 (understanding): cache memory is faster than main memory so the more that can be stored in cache memory the less frequently the main memory needs to be accessed;

1 mark for AO1 (knowledge): (increase the) word length;
1 mark for AO1 (understanding): larger word size means that the processor can process more bits in one go;

1 mark for AO1 (knowledge): (change the) type of cache memory;
1 mark for AO1 (understanding): some types of cache memory can be accessed faster;
A. using memory with a faster access speed

1 mark for AO1 (knowledge): (increase the) number of general purpose registers;
1 mark for AO1 (understanding): more intermediate results/variables can be kept in processor registers rather than in main memory;

1 mark for AO1 (knowledge): (increase the) address bus width;
1 mark for AO1 (understanding): enables the processor to access a larger number of main memory locations (meaning it will not need to make as much use of virtual memory this will mean that system performance is improved);
A. allows more main memory to be installed

R. How improves mark if it is not relevant for the factor stated.
NE How improves of "program will execute faster"

Note: Marks for the factor can be awarded in either the "factor" or "how improves" part of an answer

6

[13]

Q10.

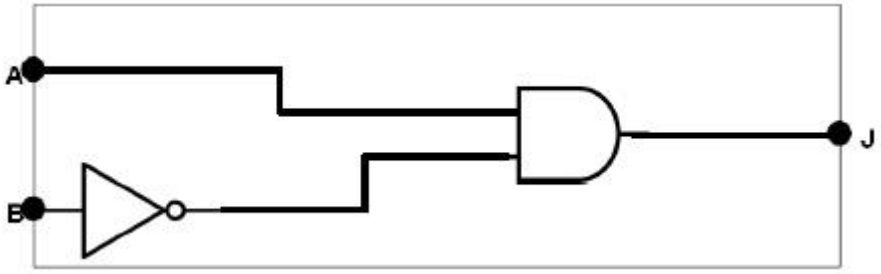
(a) (i) AND (gate);

1

(ii) NOR (gate);

1

(b) (i)



1 mark - NOT gate on input B (before any other gate);
1 mark - AND gate with inputs from A and NOT B with output connected to J;

A. 1 mark - for circuit with just AND gate with inputs from A and B connected to J

2

(ii) $\mathbf{C.H + A.\bar{J}}$

1 mark - $\mathbf{C.H}$;

1 mark - $\mathbf{A.\bar{J}}$;

1 mark for combining two previous with an OR/+ and at least one of LHS and RHS are correct;

I. K= (or other letter)

I. brackets if they will not affect expression evaluation

3

(c) $\overline{\mathbf{A.B}} + \overline{\mathbf{B+C}}$

$\bar{\mathbf{A}} + \bar{\mathbf{B}} + \bar{\mathbf{B}}.\bar{\mathbf{C}}$ – use of De Morgan's (twice)

$\bar{\mathbf{A}} + \bar{\mathbf{B}}.(\mathbf{1} + \bar{\mathbf{C}})$ – factorising

$\bar{\mathbf{A}} + \bar{\mathbf{B}}$ – from use of 1+X=1

$\overline{\mathbf{A.B}}$ – final answer (from use of De Morgan's)

Alternative answer:

$\overline{\mathbf{A.B}} + \overline{\mathbf{B+C}}$

$\overline{\mathbf{A.B}.(\mathbf{B+C})}$ – use of De Morgan's

$\overline{\mathbf{A.B.B} + \mathbf{A.B.C}}$ – expansion of bracket

$\overline{\mathbf{A.B} + \mathbf{A.B.C}}$ – from use of B.B=B

$\overline{A.B.(1+C)}$ – factorising

$\overline{A.B}$ – final answer (from use of 1+C=1)

Mark as follows
The above examples show two methods of simplifying and identify the identities used – there are other ways of simplifying the expression

3 marks should be awarded if the final answer is correct and there is evidence of good sound working.
2 marks should be awarded if the final answer is wrong/not achieved but evidence of good sound working.
2 marks should be awarded if the final answer is correct with some good working but the working also has incorrect use of identities
1 mark should be awarded if there is evidence of one correct use of an identity or simplification process
1 mark should be awarded if correct final answer on its own or with incorrect working

3

[10]

Q11.

(a) **Marks are for AO1 (knowledge)**

A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

1 mark: Table completed correctly;
1 mark: AND gate symbol drawn;

2

(b) **Marks are for AO2 (apply)**

A.B.(A + B)
A.B.A + A.B.B ; [expansion of brackets]
B.A + A.B ; [use of A.A = A]
A.B ; [use of A + A = A]

1 mark: Final answer: A.B;
Max 2 for working

3

(c) (**Marks are for AO2 (apply)**

X + Y).(X + NOT Y)

XX + X(NOT Y) + XY + Y(NOT Y) ; [expansion of brackets]
X + X(NOT Y) + XY ; [use of X.X = X or use of Y(NOT Y) = 0]
X (1 + NOT Y + Y) ; [use of 1 + X = 1]

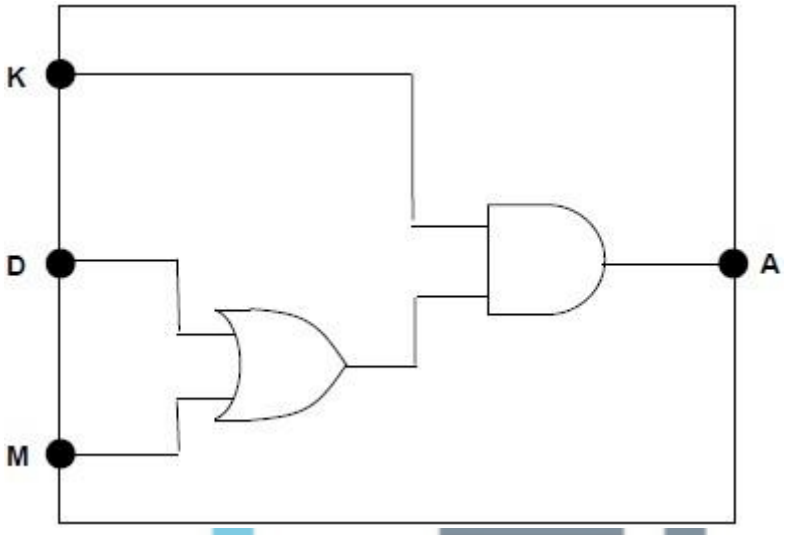
1 mark: Final answer - X;
Max 2 for working

3

[8]

Q12.

(a) **All marks AO2 (apply)**



1 mark: inputs D and M connected to an OR gate;
1 mark: inputs K and output of OR gate connected to AND gate plus output connected to A;
A a logically equivalent circuit

2

(b) **All marks AO2 (apply)**

A = (D + M) · K
1 mark: D + M somewhere in expression, even if full expression incorrect
1 mark: fully correct expression
A A logically equivalent expression

2

(c) **1 mark for AO1 (understanding), 1 mark for AO2 (application) and 1 mark for AO1 (knowledge)**

AO1 (understanding):1 mark: Flip-flop will store the state of its input / / Flip-flop acts as memory;

AO2 (application):1 mark: Insert into circuit between the output of the OR gate and the AND gate / / after the AND gate;

AO1 (knowledge):1 mark: Clock signal / / trigger / / signal to indicate when the value (of the input) should be stored / read;

3

[7]

Q13.

(a)

Input A	Input B	Output
0	0	1
0	1	1
1	0	1
1	1	0

One mark for having correct values in Output column;

1

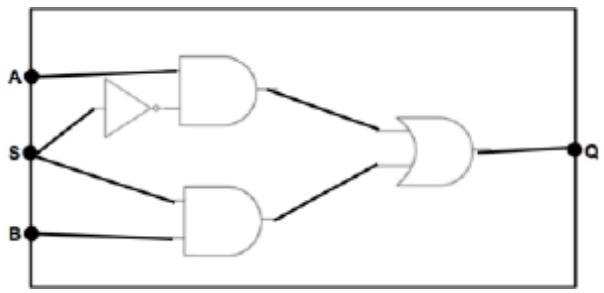
(b) (i)

S	A	B	$\bar{S}$	A.$\bar{S}$	B.S	Q
0	0	0	1	0	0	0
0	0	1	1	0	0	0
0	1	0	1	1	0	1
0	1	1	1	1	0	1
1	0	0	0	0	0	0
1	0	1	0	0	1	1
1	1	0	0	0	0	0
1	1	1	0	0	1	1

Marking:
One mark for the **A.$\bar{S}$** column being correct;
One mark for the **B.S** column being correct;
The final **Q** column should follow through from the previous two columns as an OR statement;

3

(ii)



One mark for NOT gate with input from S;
A just a circle on AND gate input from S

One mark for AND gate with input from NOT S and A;
A if no NOT gate from S

One mark for AND gate with input from B and S;

One mark for output from AND gates going into OR gate with output connect to Q;

4

(iii) A multiplexor selects one of several input lines / wires and forwards / duplicates the Boolean value on this one line onto a single line / wire;

If S is 1 then input B is output otherwise input A is output // if S is 0 then input A is output otherwise input B is output;

Note:
1 can be mapped to on / true / high
0 can be mapped to off / false / low

MAX 1

[9]

Q14.

(a) OR gate

Input A	Input B	Output
0	0	**0**
0	1	**1**
1	0	**1**
1	1	**1**

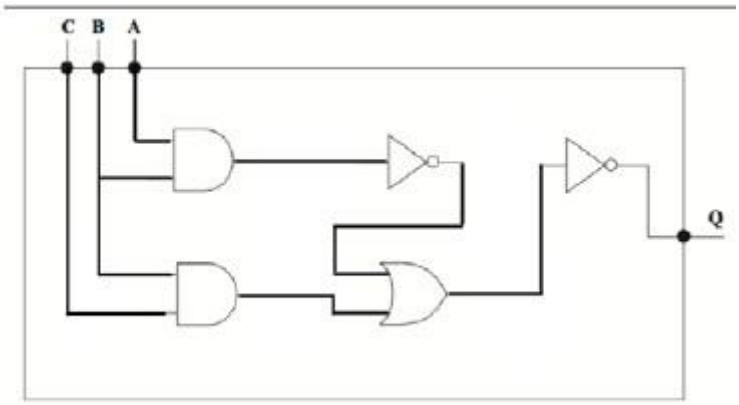
NAND gate

Input A	Input B	Output
0	0	**1**
0	1	**1**
1	0	**1**
1	1	**0**

1 mark for correct output OR gate;
1 mark for correct output NAND gate;

2

(b)



1 mark for inputs A and B connected to AND gate;
1 mark for inputs B and C connected to AND gate;
1 mark for output of AND (A,B input) as only connection going to NOT gate;
1 mark for output of NOT gate plus the AND gate (B,C input) going to OR gate;
1 mark OR gate as only connection going to NOT gate and output only connection to Q;

5

(c) **MAX 2 if working out is not logically sound**

Example 1:

$\overline{\overline{\mathbf{A}} + \overline{\overline{\mathbf{B}}} + \mathbf{B}.\overline{\mathbf{A}}}$

$\mathbf{A}.\mathbf{B} + \mathbf{B}.\overline{\mathbf{A}}$
Having applied De Morgan's correctly;

$\mathbf{B}.(\mathbf{A} + \overline{\mathbf{A}})$
Having factorised;

Final answer: **B** ;

Example 2:

$\overline{\overline{\mathbf{A}} + \overline{\overline{\mathbf{B}}} + \mathbf{B}.\overline{\mathbf{A}}}$

$\overline{(\overline{\mathbf{A}} + \overline{\mathbf{B}}).(\overline{\mathbf{B}} + \mathbf{A})}$
Having applied De Morgan's correctly;

$\overline{\overline{\mathbf{A}}.\overline{\mathbf{B}} + \overline{\mathbf{A}}.\mathbf{A} + \overline{\mathbf{B}}.\overline{\mathbf{B}} + \overline{\mathbf{B}}.\mathbf{A}}$
Expanded bracket;

$\overline{\overline{\mathbf{A}}.\overline{\mathbf{B}} + \mathbf{0} + \overline{\mathbf{B}} + \overline{B}.A}$
Simplified elements

$\overline{\overline{\mathbf{A}}.\overline{\mathbf{B}} + \overline{\mathbf{B}}}$
Having used C + C.D = C to simplify

$\overline{\overline{\mathbf{B}}}$
Having used C + C.D = C to simplify again

Final answer: B ;

Truth Table Answer

A	B	$\overline{\overline{A}+\overline{B}}$	$B.\overline{A}$	$\overline{\overline{A}+\overline{B}}+B.\overline{A}$
0	0	0	0	0
0	1	0	1	1
1	0	0	0	0
1	1	1	0	1
		X	**Y**	**Z**

1 mark for both columns marked X and Y above; (column X could be labelled **A.B**)
1 mark for final column Z;
1 mark for final answer: B;

3

[10]

Q15.

(a) AND;
NOR;
XOR; **A** EXOR // EOR // NEQ // exclusive OR;

3

(b) (i) B

1

(ii) B

1

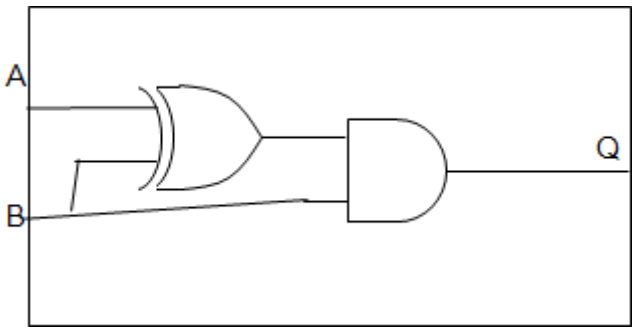
(iii) 0;;

Award 1 mark if De Morgan's has been applied once correctly but candidate does not end up simplifying to 0

Example: $\overline{B+(\bar{A}+\bar{B})}$
Example: $\bar{B}.(A.B)$

2

(c)



Inputs A and B connected to an XOR gate;

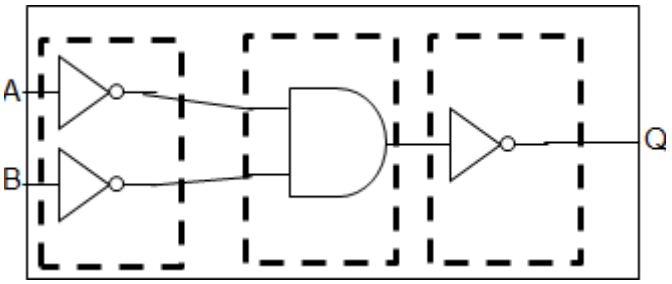
Input from B and output of XOR gate connected to an AND gate with output going to Q;

2

[9]

Q16.

(a)



1 mark – logic of first part satisfies NOT A, NOT B;
1 mark – inputs into an AND gate;
1 mark – output from AND gate passes through a NOT gate and connected to Q;

3

(b)

A	B	A + B
0	0	0
0	1	1
1	0	1
1	1	1

1 mark for correct A + B column;

A	B	$\overline{A}$	$\overline{B}$	$\overline{A}.\overline{B}$	$\overline{\overline{A}.\overline{B}}$
0	0	1	1	1	0
0	1	1	0	0	1
1	0	0	1	0	1
1	1	0	0	0	1

1 mark for columns $\overline{A}$ and $\overline{B}$ column being correct;
1 mark for $\overline{\overline{A}.\overline{B}}$ column being correct;
1 mark for $\overline{A}.\overline{B}$ column being correct;

Note: Can follow through into $\overline{A}.\overline{B}$ column from previous two

4

(c) De Morgan's (law);

1

(d) **Mark allocation:**
One mark for taking either A, NOT C or A AND NOT C outside of brackets to produce a correct expression;
One mark for eliminating B in a valid way;
One mark for correct final answer;

Example One:
$A.B.\overline{C} + A.\overline{C}$

$A\ (B.\overline{C} + \overline{C})$ - taking A outside of brackets;

$A\ (\overline{C}(B + 1))$ $(B + 1) = 1$
Simplifying to remove B using $B + 1 = 1$;

$B.\overline{C} + \overline{C} = \overline{C}$
Simplifying to remove B using $B.\overline{C} + \overline{C} = \overline{C}$;

A $A(\overline{C}\ (B + 1)) \longrightarrow A.\overline{C}$;

Final answer $A.\overline{C}$

Example Two:

$A.B.\overline{C} + A.\overline{C}$

$A.\overline{C}(B + 1)$ – taking outside of brackets;

$(B + 1) = 1$; - simplifying to remove B

A $A.\overline{C}(B + 1) \longrightarrow A.\overline{C}$

Final answer $A.\overline{C}$

Truth Table Method

A	B	C		$A.\overline{C}$	$A.B.\overline{C} + A.\overline{C}$
0	0	0		0	0
0	0	1		0	0
0	1	0		0	0
0	1	1		0	0
1	0	0		1	1
1	0	1		0	0
1	1	0		1	1
1	1	1		0	0

(student answer may have more columns than this)

A mark for having correct column for A.B.$\overline{C}$ + A.$\overline{C}$;
A mark for having correct column for A.$\overline{C}$;
Final answer A.$\overline{C}$

3

[11]

Q17.

(a)

AND Gate		
Input X	**Input X**	**Output Q**
0	0	0
0	1	0
1	0	0
1	1	1

XOR Gate		
Input X	**Input X**	**Output Q**
0	0	0
0	1	1
1	0	1
1	1	0

1 mark for each of the output columns

2

(b) (i) $(L \oplus R).\ \overline{U}$

[Brackets are not necessary]

1 mark for use of correct operands (L,R,U);
1 mark for use of XOR with L,R;
1 mark for NOT U anded with other part;

alternative: $(L + R).\ (\overline{L.R}).\overline{U}$

1 mark for use of correct operands (L,R,U);
1 mark for alternative XOR expression;
1 mark for AND NOT U;

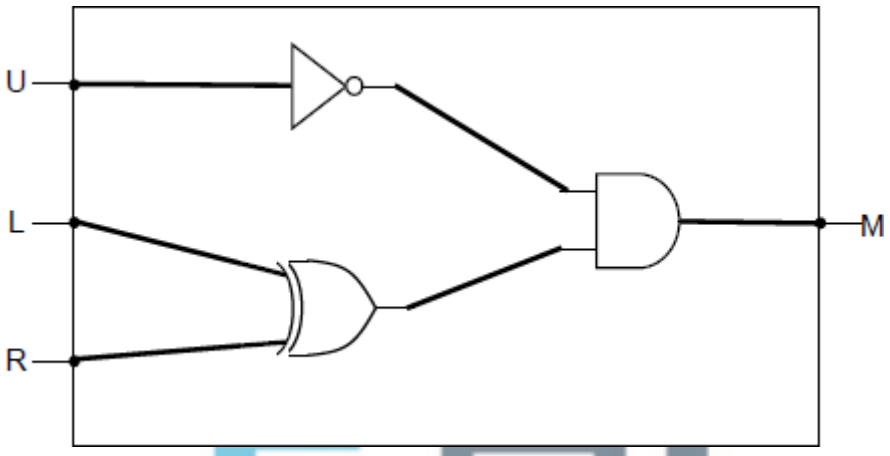
alternative: $(L.\overline{R} + \overline{L}.R).\overline{U}$

1 mark for use of correct operands (L,R,U);
1 mark for alternative XOR expression;
1 mark for AND NOT U;

Acceptable notation for symbols
~ for NOT
X.Y allow X AND Y, XэY,X)Y, XY
*X+Y allow X OR Y, X(Y, X*Y*

3

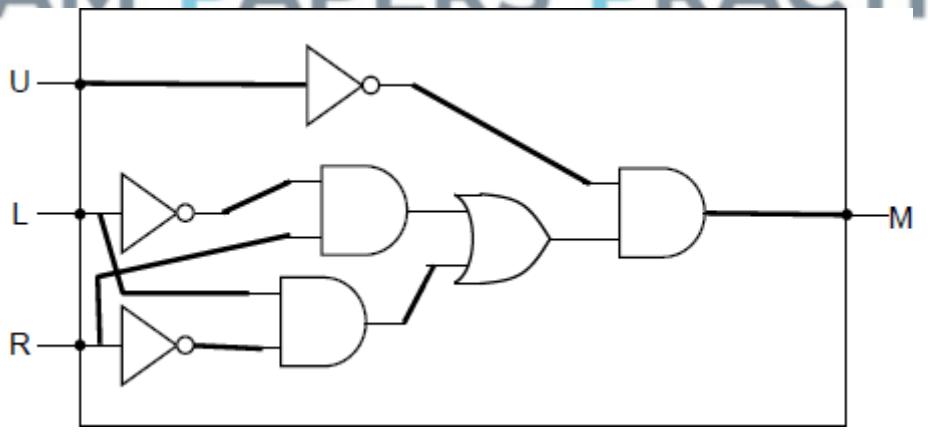
(ii)



L, R connected to XOR gate;
U connected to NOT gate;
Output of a two input AND gate connected to M;

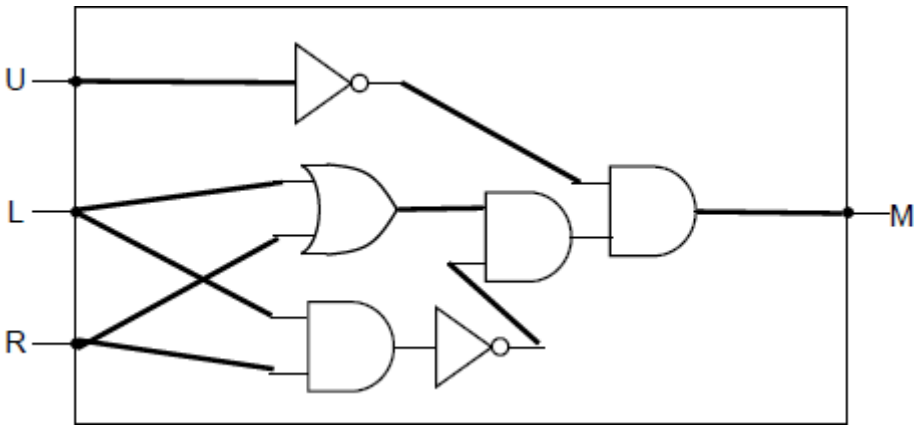
Max 2 if circuit does not reflect the correct logic

Alternative :



U connected to NOT gate;
Correct gates used for L and R before last AND gate;
Output of a two input AND gate connected to M;

Alternative :



Marked as above alternative.

3

(c) **Solution 1:**

$Q = \overline{\overline{A}.(B.A)}$ [Application of De Morgan's Law –**1 mark**]
$Q = A.B.A$ [allow simplification of double nots at same time]
[Simplification of A.A to A –**1 mark**]
$Q = A.B$ [Correct solution – **1 mark**]

Solution 2:

$Q = \overline{A} + (\overline{\overline{B} + \overline{A}})$ [Application of De Morgan's Law –**1 mark**]
$Q = \overline{\overline{A} + \overline{B} + A}$ [allow simplification of double nots at same time]
$Q = \overline{\overline{A} + \overline{B}}$ [Simplification of NOT A OR NOT A to NOT A – **1 mark**]
$Q = A.B$ [De Morgan's again to correct solution – **1 mark**]

1 mark for De Morgan;
1 mark for simplification;
1 mark for final answer;
Other notations as for section (b)

No working marks for truth table solution (asked to use De Morgan's in question)

3

[11]

Q18.

(a) X $\oplus$ Y;

$X.\overline{Y} + \overline{X}.Y$

A alternative notations:
X XOR Y
X EOR Y
X AND NOT Y OR NOT X AND Y

Acceptable notation for symbols :
For X.Y allow X∧Y, X∩Y, XY
For X+Y allow X∨Y,XUY
For X allow ~X

1

(b) $X.\overline{Y}$;

A alternative notations : X AND NOT Y;

1

(c) (i)

Inputs		Outputs	
X	**Y**	**C**	**S**
0	0	**0**	**0**
0	1	**0**	**1**
1	0	**0**	**1**
1	1	**1**	**0**

One mark for C column;
One mark for S column;

2

(ii) Addition // adder;
A sum;

1

(d)

$(X+Y).(X+\overline{Y})$ *[Fully expanding brackets – 1 mark]*

$X.X+X.\overline{Y}+Y.X+Y.\overline{Y}$ *[Recognising X.X = X OR Y.$\overline{Y}$ = 0 –1 mark]*

$X+X.\overline{Y}+Y.X+0$ *[Taking X outside brackets – 1 mark]*

$X(1+\overline{Y}+Y)$ OR $X+X(\overline{Y}+Y)$ *X[Final Answer, 1 mark]*

Alternative Answer : (Distributive)

$(X+Y).(X+\overline{Y})=X+(Y.\overline{Y})$ *[Use of distributive law – 1 mark]*

$X+(Y.\overline{Y})=X+0$ *[Recognising Y .$\overline{Y}$ = 0 – 1 mark]*

X + 0 = X *[1 mark]*

X *[Final Answer, 1 mark]*

Alternative Answer : (De Morgan's)

$\overline{\overline{X+Y}+\overline{X+\overline{Y}}}=Q$ *[Use of De Morgan's – 1 mark]*

$\overline{X+Y}+\overline{X+\overline{Y}}=\overline{Q}$

$\overline{\overline{X}.+\overline{Y}}+\overline{\overline{X}.+\overline{Y}}=\overline{Q}$ *[Two further applications of De Morgan's]*

$\overline{X}.\overline{Y}+\overline{X}.Y=\overline{Q}$ *[Taking X outside brackets – 1 mark]*

$\overline{X}.(\overline{Y}+Y)=\overline{Q}$ *[Recognising ~Y + Y = 1 – 1 mark]*

$\overline{X}.1=\overline{Q}$ *[Recognising X.1=X – 1 mark]*

$\overline{X}=\overline{Q}$

$X=Q$ *[Final answer, 1 mark]*

Max 3 for working/method;
1 for final answer
X on own with no working gains 1 mark.

Max 4

[9]

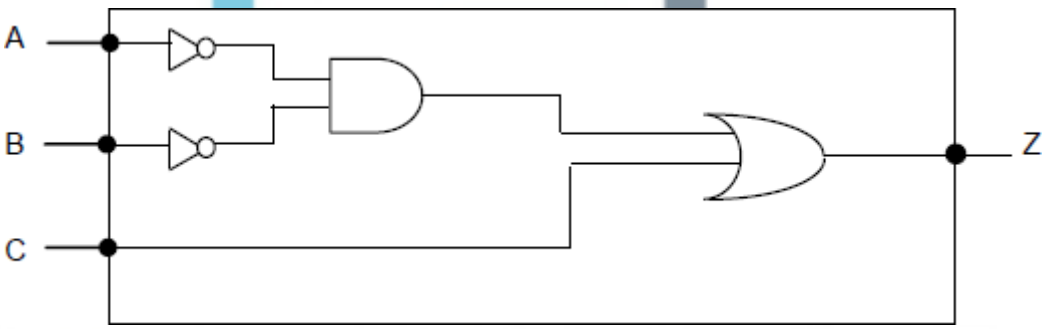
Q19.

(a)

NAND	NOR
1	1
1	0
1	0
0;	0;

2

(b)



1 mark for NOT gates on both A and B;
1 mark for AND with inputs from $\overline{A}$ *and* $\overline{B}$*;*
A inputs from A and B
1 mark for OR gate with inputs from AND gate output and C and output connected to Z;

3

(c) $\overline{(A.B)}+\overline{(A.\overline{B})}$

$(\overline{A}+\overline{B})+(\overline{A}+B)$; ; *2 marks – 1 each for De Morgans rule for each side of the central OR (award the mark for right hand expression, even if double NOT over B is not cancelled)*

$\overline{A}+\overline{B}+B$ Recognising NOT A OR NOT A is NOT A, and producing a correct expression

$\overline{A}$*+1; Recognising B or NOT B is 1*

Final answer 1 ;

Alternative answer

$\overline{\overline{(A.B)}.\overline{(A.B)}}$; Application of De Morgan's to entire expression

$\overline{(A.B).(A.\overline{B})}$; Cancellation of NOTs; 1 mark – De Morgans on entire expression

$\overline{\overline{A.B}.\overline{B}}$ Recognising A and A is A

$\overline{A.0}$ Recognising B ANDed with its complement is 0

$\overline{0;}$ Recognising 0 AND anything is 0

Final answer 1 ;

Note: Marks can be awarded for the skills above if seen but Max 3 (out of 4) for whole question if working has errors in it

A T, True for 1 and F, False for 0
A alternative notations :

- For X.Y allow X AND Y, X ∧ Y,X∩Y, XY
- For X+Y allow X OR Y, X v Y, X U Y
- For $\overline{X}$ allow NOT X, ¬X

Or by truth table M = marking point

			M		M	M	M	
A	B	A.B	$\overline{A.B}$	$\overline{B}$	$A.\overline{B}$	$\overline{A.\overline{B}}$	$\overline{A.B}$ + $\overline{A.\overline{B}}$	1
0	0	0	1	1	0	1	1	
0	1	0	1	0	0	1	1	
1	0	0	1	1	1	0	1	
1	1	1	0	0	0	1	1	

Max 3 for stages, 1 for final answer

4

[9]

Q20.

$\overline{(\overline{A}.\overline{B})}$ becomes A + B ;
A (A+B);
A A OR B;
B+ B.$\overline{C}$ becomes B ;
A B+ A. $\overline{B}$ becomes A ;
A (B+1) becomes A ;

1 mark for each

[4]

Q21.

(a)

OR Gate		
Input A	Input B	Output Q
0	0	**0**
0	1	**1**
1	0	**1**
1	1	**1**

1 mark

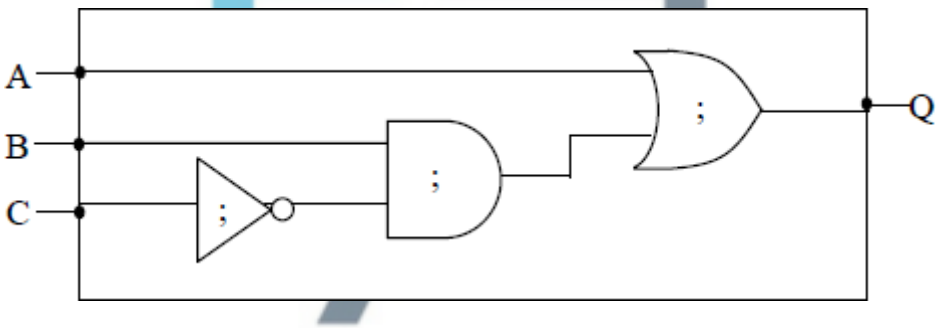
XOR Gate		
Input A	Input B	Output Q
0	0	**0**
0	1	**1**
1	0	**1**
1	1	**0**

1 mark

1 mark for each correct output column
A True for 1, False for 0

2

(b)



1 mark for NOT gate correctly linked to input C;
1 mark for AND gate correctly linked to B and $\overline{C}$ as input;
A if AND gate linked directly to C
1 mark for OR gate with inputs from A and the output of an AND gate and output connected to Q;

3

(c) **Algebraic solution:**

B.(A + $\overline{B}$)
B.A + B. $\overline{B}$ [*1 mark for expansion of brackets*]
B.A + 0 [*1 mark for identifying that B.*$\overline{B}$ *= 0*]
B.A [*1 mark for correct answer*]

Truth table solution:

		X	Y	Z
A	B	$\overline{B}$	$A+\overline{B}$	$B\cdot(A+\overline{B})$
0	0	1	1	0
0	1	0	0	0
1	0	1	1	0
1	1	0	1	1

1 mark for both columns X and Y correct
1 mark for column Z correct
1 mark for correct answer (B.A)

Any other method:
If student has used any other method to arrive at correct answer then award marks as follows:
1 mark for correct answer, no working out
2 marks for correct answer with working out, not all steps shown.
3 marks for correct answer with all steps of working out shown.

A True for 1, False for 0
A alternative notations :

- For X.Y allow X AND Y, X∧Y ,X∩Y, XY
- For X+Y allow X OR Y, X∨Y , XUY
- For $\overline{X}$ allow NOT X, ¬X

3

[8]

Q22.

Algebraic Solution:

Method 1	**Method 2**
+ A = + + A = 1 + = 1	+ A = = = = 1

1 mark for an application of a DeMorgan's law
1 mark for realisation that A + $\overline{A}$ + = 1 + or = (must be written in method, not just inferred that student has done this if arrives at correct answer)
1 mark for correct answer

Truth table solution:

		X	Y	Z
A	B	$A \cdot B$	$\overline{A \cdot B}$	$\overline{A \cdot B} + A$
0	0	0	1	1
0	1	0	1	1
1	0	0	1	1
1	1	1	0	1

1 mark for column Y correct
1 mark for column Z correct
1 mark for correct answer

Any other method:
If student has used any other method to arrive at correct answer then award marks as follows:
1 mark for correct answer, no working out
2 marks for correct answer with working out, not all steps shown.
3 marks for correct answer with all steps of working out shown.

A True for 1, False for 0
A alternative notations :

- For X.Y allow X AND Y, X∧Y ,X∩Y, XY
- For X+Y allow X OR Y, X∨Y , X∪Y
- For $\overline{X}$ allow NOT X, ¬X

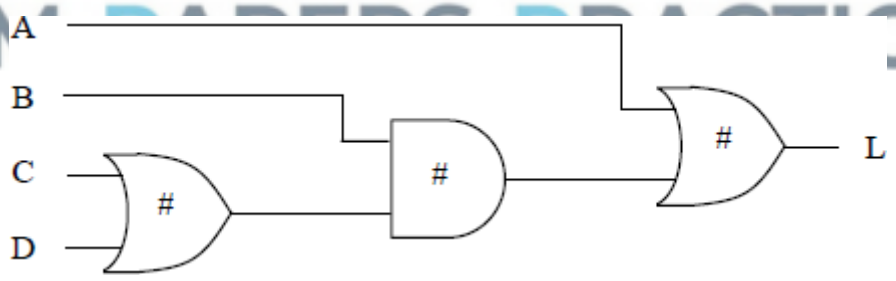
[3]

Q23.

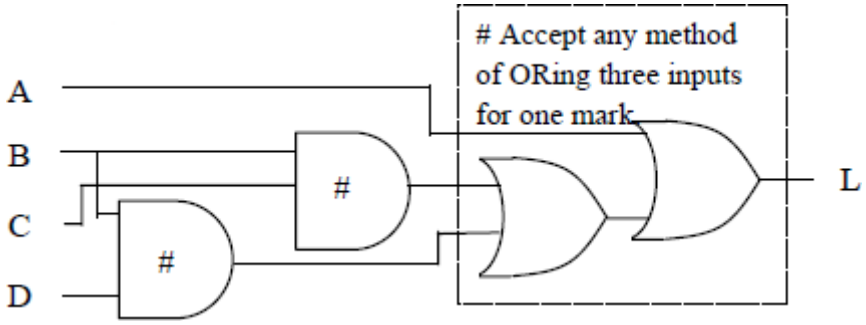
(a) NOR (Gate)
I case of answer i.e. nor is allowed

1

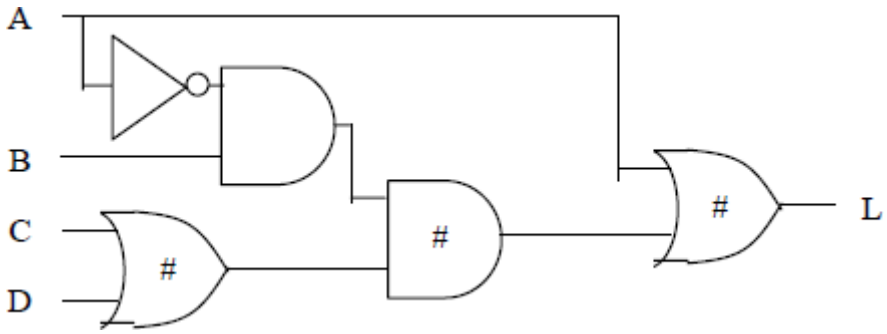
(b) (i) Solution 1:



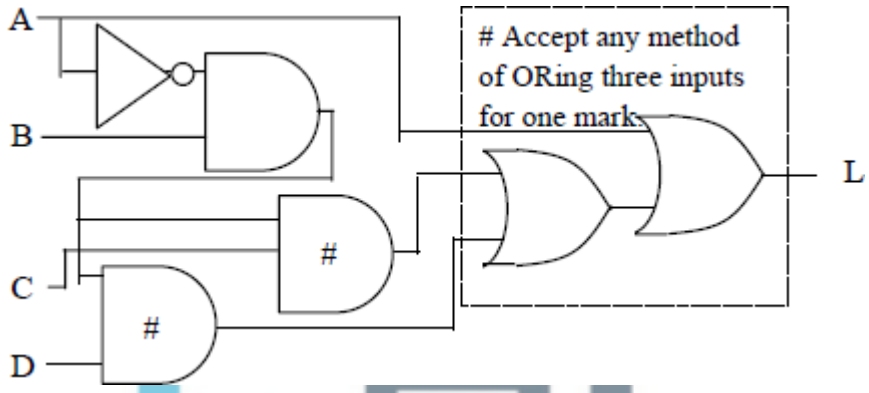
Solution 2:



Solution 3 (solution 1 plus check for A off):



Solution 4 (solution 2 plus check for A off):



1 mark for each correctly linked gate that is marked with a #

A 3-input OR gate
P1 for any unnecessary gates in a solution that would otherwise get 3 marks.
P1 for any solution that would not correctly implement the logic but would otherwise get 3 marks.

Mark from left to right until first mistake encountered then from right to left. When marking left to right award 1 mark for each gate correctly connected to its inputs. When marking right to left award 1 mark for each gate correctly connected to its output.

3

(ii) A + B.(C+ D)
A + B.C+ B.D
A + $\overline{A}$.B. (C+ D)
A + $\overline{A}$.B.C+ $\overline{A}$.B.D

A Insertion of extra brackets that do not affect logic of expression
Note: Expression does not need to match diagram drawn in (i).
A alternative notations :

- For X.Y allow X AND Y, X ∧ Y , X ∩ Y, XY
- For X+Y allow X OR Y, X ∨ Y , X ∪ Y
- For $\overline{X}$ allow NOT X, ¬X

1

(c) **Algebraic Solution:**

$\overline{\overline{A} + \overline{B}}$ + B.$\overline{A}$ [Application of DeMorgan's Law *1 mark*]

A.B + B.$\overline{A}$ [Common term B taken out *1 mark*]

B.(A + $\overline{A}$) // B.1

B [Correct answer *1 mark*]

A alternative notations :

- For X.Y allow X AND Y, X ∧Y , X ∩ Y, XY
- For X+Y allow X OR Y, X∨ Y , X∪Y
- For X allow NOT X, ¬X

Truth Table Solution:

				X	Y	Z
A	B	$\overline{A}$	$\overline{B}$	$\overline{\overline{A}+\overline{B}}$	$B \cdot \overline{A}$	$\overline{\overline{A}+\overline{B}}+B \cdot \overline{A}$
0	0	1	1	0	0	0
0	1	1	0	0	1	1
1	0	0	1	0	0	0
1	1	0	0	1	0	1

1 mark for both columns X and Y correct
1 mark for column Z correct
1 mark for correct answer (B)

A Rightmost column labelled as L or Q

3

[8]

Q24.

(a)

AND

Input A	Input B	Output
0	0	**0**
0	1	**1**
1	0	**1**
1	1	**1**

OR

Input A	Input B	Output
0	0	**0**
0	1	**0**
1	0	**0**
1	1	**1**

1 mark per correct table

2

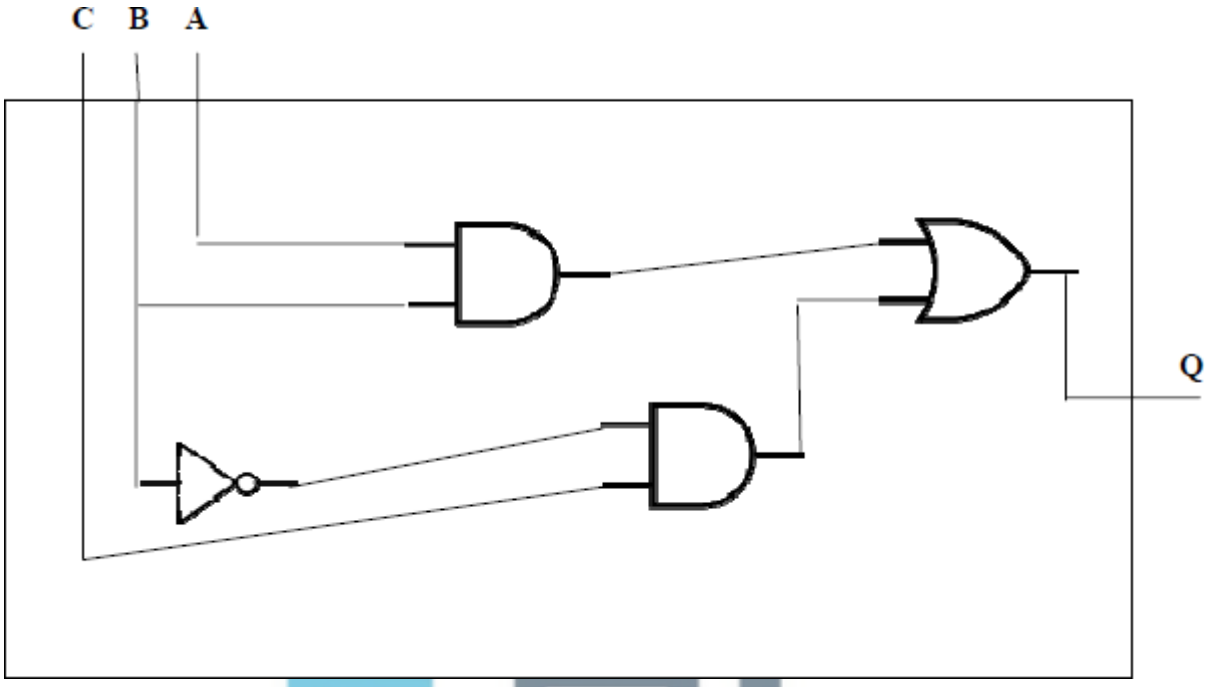
(b) (i) Q = A.B + C.$\overline{B}$

1 mark for A.B or for C.$\overline{B}$
2 marks for A.B + C.$\overline{B}$

A AND instead of .
A OR instead of +

2

(ii) *1 mark for each gate with correct inputs;;;;*
Allow two lines from B



4

[8]

Examiner reports

Q1.

The most frequent loss of marks on this question part was for linking both NOT A and NOT B with an OR gate. This demonstrated that a large number of students do not appear to be aware of the order of precedence between AND and OR.

Q2.

Most commonly students did not know the identity between $\overline{A} \cdot B + \overline{B} \cdot A$ and $A \oplus B$. Prior to this stage of the calculation, the most common error was students misapplying De Morgan's Law. This led to an incorrect algebraic statement which led to students being unable to access later mark points.

Q3.

This is the first time that students have been asked to produce a proof that two Boolean expressions are equivalent. It was well tackled, with over 40% of students achieving full marks. A common mistake was to believe that $D + \overline{D} = 0$.

Some responses were difficult to mark as the way that students laid them out made it unclear what order they had done things in. It is particularly important when presenting a proof that the examiner can see what steps the student took and in what order these were made. In other responses, students would miss out steps, making jumps in their working that were not convincing enough to be a proof.

Q4.

It was pleasing to see that the majority of students tackled this question and a large number did so successfully using a number of approaches. The most common mistakes included not identifying Y AND NOT Y as being equal to 0, or not fully simplifying to a final answer. Some students dropped marks by making leaps which, whilst arithmetically correct, were not Boolean identities and could not be followed directly. In this case it is impossible to distinguish between correct understanding and a lucky guess.

Q5.

(a) This question part was well tackled with over three quarters of students drawing a fully correct logic circuit. If students make a mistake whilst drawing a logic circuit and they cannot correct it in a clear way then they are advised to redraw it on a new sheet of paper as it can be difficult to discern what type of gate the student had drawn if, for example, an AND gate is drawn on top of an OR gate.

(b) This question part was well tackled. Students need to be aware of the significance of brackets as the expression (A.B).(C+D) is not logically equivalent to A.B.C+D as the AND (.) operation has a higher order of precedence than OR (+). Three quarters of students achieved both available marks.

Q6.

Most students achieved some marks for this question part but only a fifth achieved full marks. The most commonly made mistake was to incorrectly apply the identity $A+\overline{A}=1$ to the subexpression $\overline{A}+A \cdot (A+B)$ which failed to recognise that this could not be done because of the order of precedence of AND (.) and OR (+). Another mistake made by

some students was to cancel NOTs when they could not be cancelled, for example believing that the NOTs in ($\overline{B}\cdot\overline{C}$) could be cancelled with the longer NOT that related to the entire expression.

Q8.

This question was about Boolean algebra.

While a number of very good answers to this question were seen, candidates often struggled to apply de Morgan's law correctly within an expression.

Q9.

This question was about computer systems, computer organisation and architecture.

Parts (a) and (d) were generally well-answered. Candidates often were not able to simplify the Boolean expressions in parts (b) and (c), with a wide variety of incorrect answers seen. A good range of correct factors were seen in the answers to part (f), a common response that obtained no marks, as it had already been given in the question, was to increase the number of cores.

Q10.

This question was answered well by students. The majority of students could identify the logic gates correctly and could also draw the logic circuit. When drawing a logic circuit diagram students do need to be careful to connect up to the input and output points.

The most challenging part was (c) which asked students to simplify a Boolean expression. The correct use of De Morgan's is still a challenge for some students when the expression has a few ways that it could be applied. A common mistake is to switch all of the signs across the whole of the expression at once.

Q13.

Students continue to be well prepared for questions based around logic gates and circuit drawing. The majority of students secured high marks for all question parts. When drawing circuits a few students swapped over the AND and OR symbols. It was also hard, occasionally, to spot any difference between the drawing of AND and OR symbols.

Q14.

Overall, candidates continue to demonstrate a good understanding of logic and Boolean algebra.

(a) For this part candidates demonstrated a secure knowledge of the basic logic gates with around 75% achieving the two marks. A few candidates struggled with the NAND gate.

(b) The majority of candidates secured full marks for this part which asked for a logic circuit to be connected up. It was pleasing to see that candidates could identify the symbols for each logic gate and follow a relatively complex equation.

The simplification of a Boolean expression remains a challenging part of the paper with around a third of students not managing to secure any marks. Completing a logic table perhaps enabled weaker students to pick up some of the marks and should be a skill candidates can switch to if they find Boolean algebra too

challenging. A third of candidates secured all of the marks and from their working it was clear that they could apply De Morgan's laws effectively and then factorise out a common element.

Q15.

The majority of students performed well across this question but it was the Boolean simplification parts that caught out some students.

Part (a) had over half of all students gaining full marks for identifying the logic gates for each truth table correctly. The NOR gate proved to be the most challenging truth table to decipher. The three simplification parts appeared to get progressively harder for students working through the paper. It is to be noted again that students do appear to understand that a law of De Morgan needs to be used but they apply it across the whole expression rather than carefully separating it into a left and right part with one operation in the middle.

Part (c) had over 80% of students securing full marks and was answered well. Mistakes came only from students placing the gates in the wrong order or drawing gates incorrectly.

Q16.

A large number of students secured all 3 marks for drawing out the logic circuit required for part (a) and it was also pleasing to see the neatness of the majority of the diagrams. Mistakes identified included connecting pairs of not gates to each input.

The truth tables in part (b) were also answered well with the majority of students securing all of the marks.

Given that the students performed very well with the early parts of this question, it was perhaps surprising to see the number of students who did not secure any marks in part (d). On this paper, students were free to use any method to simplify the Boolean expression and those that tried a truth table method, in general, were able to pick up at least one mark. It is obvious that some of the weaker students just attempt a simple guess at the final answer because in previous papers it has been just A, for example. It also appeared that some students tried to tackle this question by applying De Morgan's in many different ways, not realising that there are other ways to go about simplifying.

Q17.

Students are continuing to demonstrate that they can answer questions concerning logic gates and Boolean algebra. The majority could correctly fill in both of the truth tables for part (a).

Questions parts (b)(i) and (ii) had the majority of students securing 2 or 3 of the 3 marks available. Whilst it might be considered a harder skill to take some descriptive text and turn it into a logical statement, it was pleasing to see most students had a good attempt at this.

Part (c) appeared to be the most difficult section of this question and whilst students demonstrated that they might know De Morgan's law, they failed to apply it correctly. Sometimes this was obvious with a student writing out the laws next to their working. Students often switched both signs of the provided expression at once, rather than correctly separating it into two parts and therefore only changing one sign. Students who completed the De Morgan's part correctly then tended to go on and secure the other 2 marks.

Q18.

On previous papers students have always done well in identifying logic gates but on this paper only around half correctly identified the XOR gate by writing a correct expression.

Over 90% of students correctly wrote the second expression and this highlights the case for further work on XOR gates. Based on the evidence seen in this and previous papers, students seem to be less familiar with XOR, NAND and NOR gates than OR, AND and NOT gates.

The truth table was completed well by the majority of students with only a small number of students not scoring any marks.

Identifying the arithmetic function was asked to probe students' understanding and it was pleasing to see students supplying the correct answer of addition with some students recognising that the circuit was a half-adder.

Part (d) was asked in order to test the students' ability to simplify a Boolean expression using known identities. Students went down various routes to attempt to simplify the expression with expanding the brackets being the most common. It was pleasing to see a group of students solve by starting with the distributive identity and this usually meant that a full solution was found very quickly. It was common for weaker students just to remove completely the brackets and to then start working with the expression.

Very few students did not attempt to solve this question part using the required method. It is important to note that the specification states that students should, 'Be familiar with the use of De Morgan's laws and Boolean identities to manipulate and simplify simple Boolean expressions.' Truth tables can also be useful tools for simplification, but they only work well in quite specific circumstances and the specification requires that students are aware of how to simplify using Boolean identities.

Q19.

Part (a) asked candidates to complete truth tables for a NAND and a NOR gate. It was pleasing to see that most candidates could secure both marks for this part. A few candidates answered the wrong way around whilst others provided the truth table for a XOR gate rather than a NOR gate.

The majority of candidates scored very well in part (b) securing full marks for the correct drawing of the logic circuit. The most common mistake was to put the AND gate before the NOT. Some candidates did not understand which gates related to each operator in the equation and therefore had the AND and OR gates swapped around.

Part (c) asked candidates to simplify a Boolean expression and a variety of methods were used. Candidates were awarded marks for a method where it was clear that a required skill was being used. When showing stages of working we would encourage candidates to make sure they only perform one step at a time. Good candidates also provided the rules they were using as explanation of their method. Candidates who realized that De Morgan's law could be applied to both sides of the equation and did this correctly quite quickly secured two marks for the method. A few candidates stopped when they reached a certain position not realizing that they could simplify further. The candidates who attempted this question using a truth table method tended to also score well.

Q20.

This question focused on simplifying four short Boolean expressions, in contrast to earlier papers which required the simplification of more complex expressions. Candidates scored well on part (a) and it is clear that De Morgan's laws are now well known. Part (c) caused

fewer problems than parts (b) and (d). It does appear that candidates need more exposure to simplifying expressions. A few candidates inserted new letters into their answers for no apparent reason. Quite a few candidates gave no response.

Q21.

The question about Boolean logic, truth table and logic diagrams was answered much better than in previous years. This may be because the parts concerning drawing a logic diagram and simplifying a Boolean equation were a little more straightforward than those which had previously been asked. The truth table for an OR gate was completed more accurately than that for an EOR gate. The logic diagram often gained three marks and for the first time it was to see just three components drawn in the diagram rather than a whole series of symbols. The shapes of some of the symbols were far from ideal but those that were nearly there were accepted rather than rejected. The hardest part of the question, simplifying Boolean expression, was also the one that gained least marks. It was however gratifying to see that on the whole it was answered far better than similar questions in previous years. Candidates often left out the intermediate step we required and this was where most marks were lost. There were still some candidates who made no attempt at this question.

Q22.

This question was tackled using either truth tables or the laws of Boolean algebra, with the number of candidates using each method being approximately equal. Candidates who used the truth table method appeared to make fewer errors. Many candidates showed the correct steps, using either method, but then failed to state the final answer explicitly. Candidates using the rules of Boolean algebra often made the first step by applying De Morgan's law, but then ground to a halt. It would appear that Boolean algebra is still a topic that candidates find difficult. Often candidates would reach A OR NOT A and then make these terms completely disappear instead of equating them to '1'. Care was needed with the answer as moving the terms around to simplify it often resulted in transposition errors which lead to the wrong answer. There were many false starts with answers crossed out and the whole answer being rewritten.

Q23.

Some candidates correctly identified the truth table as representing the NOR logic gate, but there was a wide range of different responses to this question part.

The logic circuit question was well answered with many candidates getting two or three of the three available marks. Most realised that it was not necessary to NOT the A and AND it with B, although candidates were not penalised if they did this. Diagrams were usually drawn clearly.

Many candidates were able to state a correct Boolean expression that represented the logic circuit. Some introduced unnecessary brackets into the expression, but these were not penalised if they did not affect the expression's logic.

Most candidates attempted to simplify the Boolean expression by applying the laws of Boolean algebra. A smaller number constructed a truth table which was also acceptable. When using the former method, many candidates recognised that the first step was to apply DeMorgan's laws to the left hand part of the term, but fewer knew what to do after this step had been completed.

The most common mistake was to assume that A + B = A + B = A + B rather than applying De Morgan's laws. Candidates need to ensure that they explicitly show all stages of their working out. A number of candidates scored a mark for having the correct final answer and for the

application of De Morgan's law, but lost a mark for not making the other steps in the simplification clear.

Candidates who produce truth table solutions to this type of question must ensure that they state the simplified expression at the end of their solution. A few produced an accurate truth table, but failed to state the resulting expression.

Q24.

Most candidates had no difficulty completing the truth tables. It was pleasing to see that a large number of candidates correctly expressed the given scenario as a Boolean equation. A few candidates mixed up the symbols for AND and OR. Many candidates correctly completed the logic gate diagram, even if they did not write down the correct Boolean expression. Each gate that had been given the correct inputs was awarded a mark. Some candidates drew very neat diagrams and helped themselves by writing the equation on the output of each gate. A few candidates missed out on marks because they had not connected the gates to each other.