# 6.4 Logic gates Mark Scheme

## Q1.

(a) **All marks AO2 (apply)**

| Input | | | | | | Outputs | |
|---|---|---|---|---|---|---|---|
| **A** | **B** | **C** | **D** | **E** | **F** | **G** | **H** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |

**1 mark:** Column D correct or column E or column F correct
**1 mark:** Column G correct
**1 mark:** Column H correct

**Max 2** if any incorrect values in table

3

(b) **All marks AO2 (apply)**

$B \cdot C + A \cdot (B \oplus C)$

**1 mark:** $B \cdot C$ or $B \oplus C$ somewhere in expression
**1 mark:** A is ANDed with $B \oplus C$
**1 mark:** Fully correct expression
**A.** award second mark even if brackets around $B \oplus C$ are missing
**A.** use of AND, OR, XOR instead of symbols
**A.** $(\overline{B} \cdot C)+(B \cdot \overline{C})$ for $(B \oplus C)$



**If a student has written an expression but then tried to simplify it and made an error then mark the original expression that the student has written down and ignore the simplification.**

3

(c) **Mark is for AO2 (analyse)**

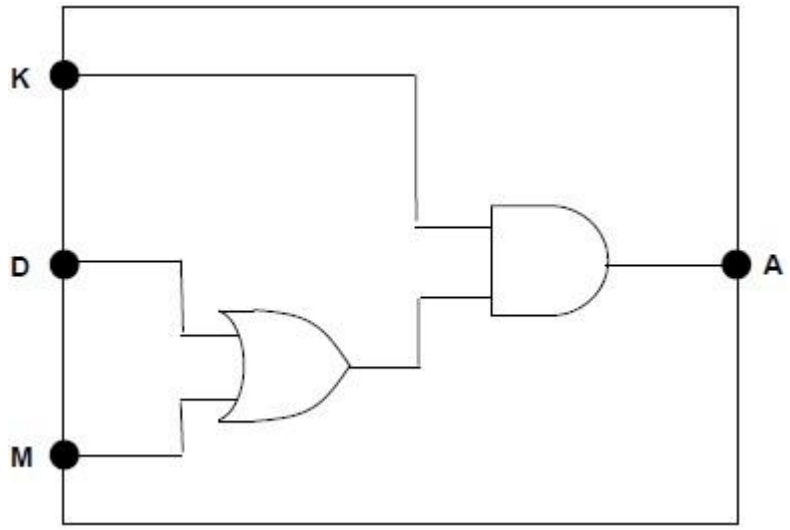
It adds together its inputs // it is a full adder circuit;
**N.E.** half-adder, adder

1

**[7]**

## Q2.

(a) **All marks AO2 (apply)**




**1 mark:** inputs D and M connected to an OR gate;
**1 mark:** inputs K and output of OR gate connected to AND gate plus output connected to A;
**A** a logically equivalent circuit

2

(b) **All marks AO2 (apply)**

A = (D + M) · K
**1 mark:** D + M somewhere in expression, even if full expression incorrect
**1 mark:** fully correct expression
**A** A logically equivalent expression

2

(c) **1 mark for AO1 (understanding), 1 mark for AO2 (application) and 1 mark for AO1 (knowledge)**

**AO1 (understanding):1 mark:** Flip-flop will store the state of its input / / Flip-flop acts as memory;

**AO2 (application):1 mark:** Insert into circuit between the output of the OR gate and the AND gate / / after the AND gate;

**AO1 (knowledge):1 mark:** Clock signal / / trigger / / signal to indicate when the value (of the input) should be stored / read;

3

**[7]**

## Q3.

(a)

| Input A | Input B | Output |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

One mark for having correct values in Output column;

1

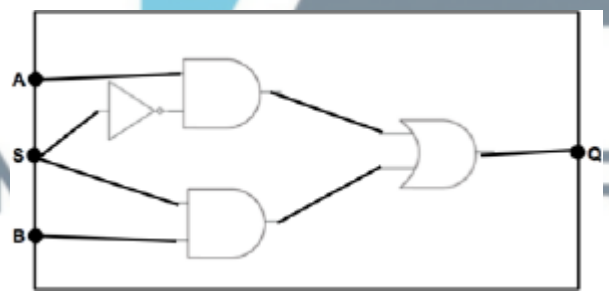
(b) (i)

| S | A | B | $\bar{S}$ | A.$\bar{S}$ | B.S | Q |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 |

**Marking:**
One mark for the **A.$\bar{S}$** column being correct;
One mark for the **B.S** column being correct;
The final **Q** column should follow through from the previous two columns as an OR statement;

3

(ii)




One mark for NOT gate with input from S;
**A** just a circle on AND gate input from S

One mark for AND gate with input from NOT S and A;
**A** if no NOT gate from S

One mark for AND gate with input from B and S;

One mark for output from AND gates going into OR gate with output connect to Q;

4

(iii) A multiplexor selects one of several input lines / wires and forwards / duplicates the Boolean value on this one line onto a single line / wire;

If S is 1 then input B is output otherwise input A is output // if S is 0 then input A is output otherwise input B is output;

Note:
1 can be mapped to on / true / high
0 can be mapped to off / false / low

**MAX 1**

**[9]**

## Q4.

(a) OR gate

| Input A | Input B | Output |
|---|---|---|
| 0 | 0 | **0** |
| 0 | 1 | **1** |
| 1 | 0 | **1** |
| 1 | 1 | **1** |

NAND gate

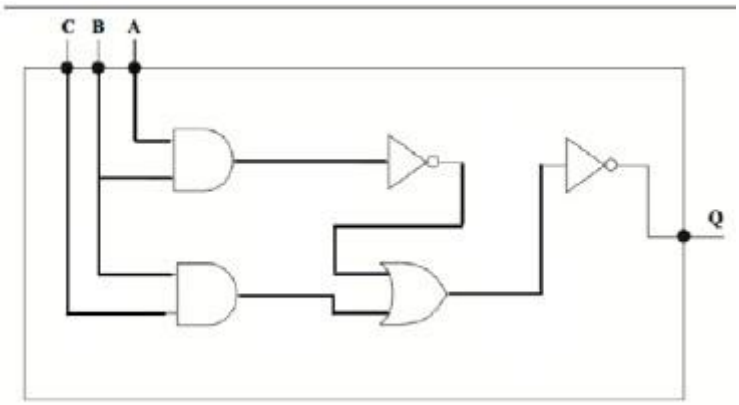
| Input A | Input B | Output |
|---|---|---|
| 0 | 0 | **1** |
| 0 | 1 | **1** |
| 1 | 0 | **1** |
| 1 | 1 | **0** |

**1 mark** for correct output OR gate;
**1 mark** for correct output NAND gate;



**2**

(b)




**1 mark** for inputs A and B connected to AND gate;
**1 mark** for inputs B and C connected to AND gate;
**1 mark** for output of AND (A,B input) as only connection going to NOT gate;
**1 mark** for output of NOT gate plus the AND gate (B,C input) going to OR gate;

**1 mark** OR gate as only connection going to NOT gate and output only connection to Q;

5

(c) **MAX 2 if working out is not logically sound**

**Example 1**:

$$\overline{\overline{\overline{A}+\overline{B}}+B.\overline{A}}$$

$$A.B+B.\overline{A}$$

Having applied De Morgan's correctly;

$$B.(A+\overline{A})$$

Having factorised;

Final answer: **B** ;

**Example 2**:

$$\overline{\overline{\overline{A}+\overline{B}}+B.\overline{A}}$$

$$\overline{(\overline{A}+\overline{B}).(\overline{B}+A)}$$

Having applied De Morgan's correctly;

$$\overline{\overline{A}.\overline{B}+\overline{A}.A+\overline{B}.\overline{B}+\overline{B}.A}$$

Expanded bracket;

$$\overline{\overline{A}.\overline{B}+0+\overline{B}+\overline{B}.A}$$

Simplified elements

$$\overline{\overline{A}.\overline{B}+\overline{B}}$$

Having used C + C.D = C to simplify

$$\overline{\overline{B}}$$

Having used C + C.D = C to simplify again

**Final answer: B ;**

***Truth Table Answer***

| A | B | $\overline{\overline{A}+\overline{B}}$ | $B.\overline{A}$ | $\overline{\overline{A}+\overline{B}}+B.\overline{A}$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 |
| | | **X** | **Y** | **Z** |

**1 mark** for both columns marked X and Y above; (column X could be labelled **A.B** )
**1 mark** for final column Z;
**1 mark** for final answer: B;

3

**[10]**

## Q5.

(a) AND;
NOR;
XOR; **A** EXOR // EOR // NEQ // exclusive OR;

3

(b) (i) B

1

(ii) B

1

(iii) 0;;

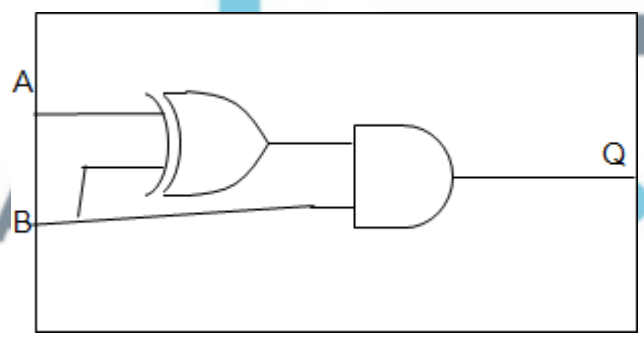
Award 1 mark if De Morgan's has been applied once correctly but candidate does not end up simplifying to 0

Example: $\overline{B + (\bar{A} + \bar{B})}$

Example: $\overline{\bar{B} . (A . B)}$

2

(c)




Inputs A and B connected to an XOR gate;

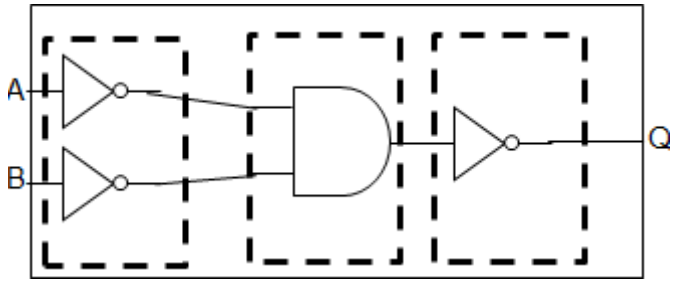
Input from B and output of XOR gate connected to an AND gate with output going to Q;

2

**[9]**

## Q6.

(a)




1 mark – logic of first part satisfies NOT A, NOT B;
1 mark – inputs into an AND gate;
1 mark – output from AND gate passes through a NOT gate and connected to Q;

**3**

(b)

| A | B | A + B |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

1 mark for correct A + B column;

| A | B | $\overline{A}$ | $\overline{B}$ | $\overline{A}.\overline{B}$ | $\overline{\overline{A}.\overline{B}}$ |
|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 |

1 mark for columns $\overline{A}$ and $\overline{B}$ column being correct;
1 mark for $\overline{\overline{A}.\overline{B}}$ column being correct;
1 mark for $\overline{A}.\overline{B}$ column being correct;

Note: Can follow through into $\overline{A}.\overline{B}$ column from previous two

**4**

(c) De Morgan's (law);

**1**

(d) **Mark allocation:**
One mark for taking either A, NOT C or A AND NOT C outside of brackets to produce a correct expression;
One mark for eliminating B in a valid way;
One mark for correct final answer;

**Example One:**
$A.B.\overline{C} + A.\overline{C}$

$A\,(B.\overline{C} + \overline{C})$ - taking A outside of brackets;

$A\,(\overline{C}(B + 1))$ $(B + 1) = 1$
Simplifying to remove B using B + 1 = 1 ;

$B.\overline{C} + \overline{C} = \overline{C}$
Simplifying to remove B using $B.\overline{C} + \overline{C} = \overline{C}$;

**A** $A(\overline{C}\ (B + 1)) \longrightarrow A.\overline{C}$;

Final answer $A.\overline{C}$

**Example Two:**

$A.B.\overline{C} + A.\overline{C}$

$A.\overline{C}(B + 1)$ – taking outside of brackets;

(B + 1 ) = 1; - simplifying to remove B

**A** $A.\overline{C}(B + 1) \longrightarrow A.\overline{C}$

Final answer $A.\overline{C}$

**Truth Table Method**

| A | B | C | | $A.\overline{C}$ | $A.B.\overline{C} + A.\overline{C}$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | | 0 | 0 |
| 0 | 0 | 1 | | 0 | 0 |
| 0 | 1 | 0 | | 0 | 0 |
| 0 | 1 | 1 | | 0 | 0 |
| 1 | 0 | 0 | | 1 | 1 |
| 1 | 0 | 1 | | 0 | 0 |
| 1 | 1 | 0 | | 1 | 1 |
| 1 | 1 | 1 | | 0 | 0 |

(student answer may have more columns than this)

A mark for having correct column for $A.B.\overline{C} + A.\overline{C}$;
A mark for having correct column for $A.\overline{C}$;
Final answer $A.\overline{C}$

3

**[11]**

## Q7.

(a)

| AND Gate | | |
|---|---|---|
| **Input X** | **Input X** | **Output Q** |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

| XOR Gate | | |
|---|---|---|
| **Input X** | **Input X** | **Output Q** |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

*1 mark for each of the output columns* **2**

(b) (i) $(L \oplus R).\overline{U}$

[Brackets are not necessary]

*1 mark for use of correct operands (L,R,U);*
*1 mark for use of XOR with L,R;*
*1 mark for NOT U anded with other part;*

alternative: $(L + R).\ (\overline{L.R}).\overline{U}$

*1 mark for use of correct operands (L,R,U);*
*1 mark for alternative XOR expression;*
*1 mark for AND NOT U;*

alternative: $(L.\overline{R} + \overline{L}.R).\overline{U}$

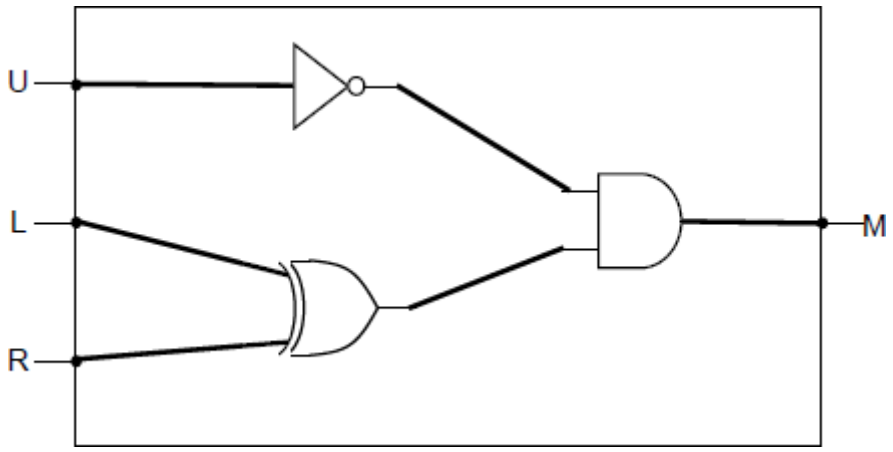
*1 mark for use of correct operands (L,R,U);*
*1 mark for alternative XOR expression;*
*1 mark for AND NOT U;*

*Acceptable notation for symbols*
*~ for NOT*
*X.Y allow X AND Y, XэY,X)Y, XY*

*X+Y allow X OR Y, X(Y, X*Y*

3

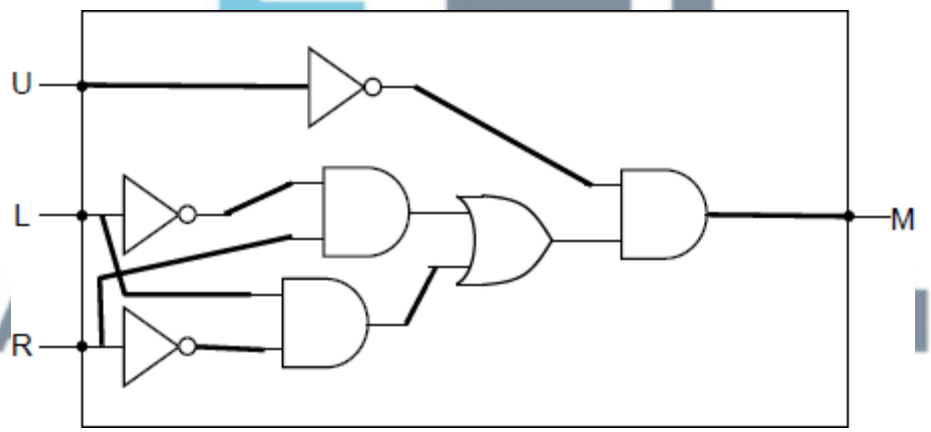
(ii)




L, R connected to XOR gate;
U connected to NOT gate;
Output of a two input AND gate connected to M;

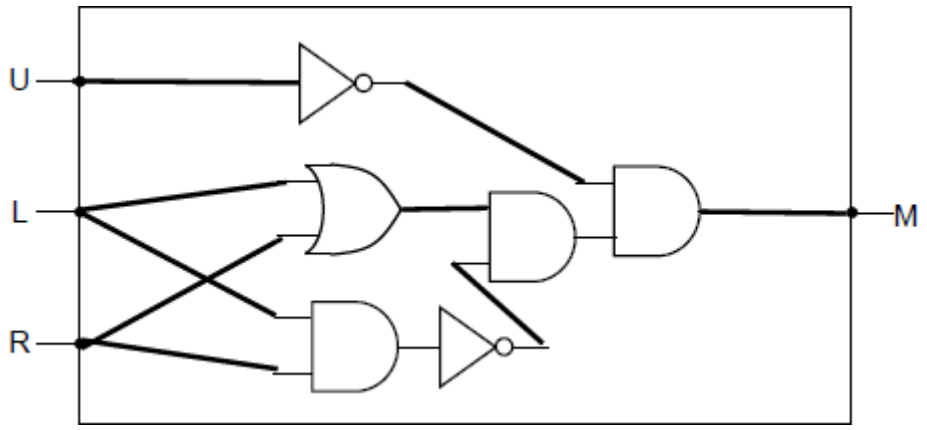
*Max 2 if circuit does not reflect the correct logic*

**Alternative :**




U connected to NOT gate;
Correct gates used for L and R before last AND gate;
Output of a two input AND gate connected to M;

**Alternative :**




Marked as above alternative.

3

(c) **Solution 1:**

$Q = \overline{\overline{A}.\ (\overline{B.A})}$ [Application of De Morgan's Law –**1 mark**]

$Q = A.B.A$ [allow simplification of double nots at same time]

[Simplification of A.A to A –**1 mark**]

$Q = A.B$ [Correct solution – **1 mark**]

**Solution 2:**

$Q = \overline{A} + (\overline{\overline{B} + \overline{A}})$ [Application of De Morgan's Law –**1 mark**]

$Q = \overline{\overline{A} + \overline{B} + \overline{A}}$ [allow simplification of double nots at same time]

$Q = \overline{\overline{A} + \overline{B}}$ [Simplification of NOT A OR NOT A to NOT A – **1 mark**]

$Q = A.B$ [De Morgan's again to correct solution – **1 mark**]



*1 mark for De Morgan;*
*1 mark for simplification;*
*1 mark for final answer;*
*Other notations as for section (b)*

*No working marks for truth table solution (asked to use De Morgan's in question)*

3

**[11]**

## Q8.

(a) $X \oplus Y$;

$X.\overline{Y} + \overline{X}.Y$

**A** alternative notations:
X XOR Y
X EOR Y
X AND NOT Y OR NOT X AND Y

*Acceptable notation for symbols :*
*For X.Y allow X∧Y, X∩Y, XY*
*For X+Y allow XvY,XUY*
*For X allow ~X*

1

(b) $X.\overline{Y}$;

**A** alternative notations : X AND NOT Y;

1

(c) (i)

| Inputs | | Outputs | |
|---|---|---|---|
| **X** | **Y** | **C** | **S** |
| 0 | 0 | **0** | **0** |
| 0 | 1 | **0** | **1** |
| 1 | 0 | **0** | **1** |
| 1 | 1 | **1** | **0** |

*One mark for C column;*
*One mark for S column;*

2

(ii) Addition // adder;
**A** sum;

1

(d)

$(X+Y).(X+\overline{Y})$ *[Fully expanding brackets – 1 mark]*

$X.X + X.\overline{Y} + Y.X + Y.\overline{Y}$ *[Recognising X.X = X OR Y.$\overline{Y}$ = 0 –1 mark]*

$X + X.\overline{Y} + Y.X + 0$ *[Taking X outside brackets – 1 mark]*

$X(1+\overline{Y}+Y)$ OR $X + X(\overline{Y}+Y)$ *X[Final Answer, 1 mark]*

**Alternative Answer : (Distributive)**

$(X+Y).(X+\overline{Y}) = X + (Y.\overline{Y})$ *[Use of distributive law – 1 mark]*

$X + (Y.\overline{Y}) = X + 0$ *[Recognising Y . $\overline{Y}$ = 0 – 1 mark]*

X + 0 = X *[ 1 mark ]*

X *[Final Answer, 1 mark]*

**Alternative Answer : (De Morgan's)**

$\overline{\overline{X+Y}} + \overline{\overline{X+\overline{Y}}} = Q$ *[Use of De Morgan's – 1 mark]*

$\overline{X+Y} + \overline{X+\overline{Y}} = \overline{Q}$

$\overline{\overline{X}.\overline{Y}} + \overline{\overline{X}.\overline{\overline{Y}}} = \overline{Q}$ *[Two further applications of De Morgan's]*

$\overline{X}.\overline{Y} + \overline{X}.Y = \overline{Q}$ *[Taking X outside brackets – 1 mark]*

$\overline{X}.(\overline{Y}+Y) = \overline{Q}$ *[Recognising ~Y + Y = 1 – 1 mark]*

$\overline{X}.1 = \overline{Q}$ *[Recognising X.1=X – 1 mark]*

$\overline{X}=\overline{Q}$

$X=Q$ *[Final answer, 1 mark]*

*Max 3 for working/method;*
*1 for final answer*
*X on own with no working gains 1 mark.*

**Max 4**

**[9]**

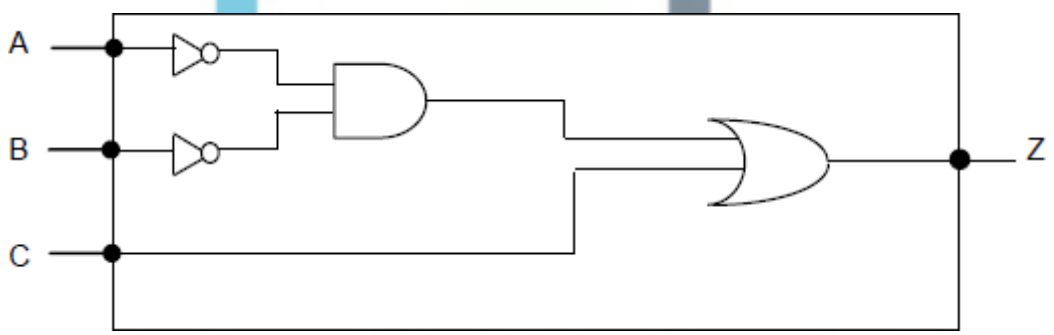
## Q9.

(a)

| NAND | NOR |
|---|---|
| 1 | 1 |
| 1 | 0 |
| 1 | 0 |
| 0; | 0; |

**2**

(b)






*1 mark for NOT gates on both A and B;*
*1 mark for AND with inputs from* $\overline{A}$ *and* $\overline{B}$*;*
**A** inputs from A and B
*1 mark for OR gate with inputs from AND gate output and C and output connected to Z;*

**3**

(c) $\overline{(\overline{A.B})}+\overline{(\overline{A.\overline{B}})}$

$(\overline{A}+\overline{B})+(\overline{A}+B)$; ; *2 marks – 1 each for De Morgans rule for each side of the central OR (award the mark for right hand expression, even if double NOT over B is not cancelled)*

$\overline{A}+\overline{B}+B$ Recognising NOT A OR NOT A is NOT A, and producing a correct expression

$\overline{A}+1$*; Recognising B or NOT B is 1*

Final answer 1 ;

**Alternative answer**

$\overline{\overline{(A.B)}.\overline{(A.\overline{B})}}$; Application of De Morgan's to entire expression

$\overline{(A.B).(A.\overline{B})}$; Cancellation of NOTs; 1 mark – De Morgans on entire expression

$\overline{\overline{A.B}.\overline{B}}$ Recognising A and A is A

$\overline{A.0}$ Recognising B ANDed with its complement is 0

$\overline{0}$; Recognising 0 AND anything is 0

Final answer 1 ;

*Note: Marks can be awarded for the skills above if seen but Max 3 (out of 4) for whole question if working has errors in it*

**A** T, True for 1 and F, False for 0
**A** alternative notations :

- For X.Y allow X AND Y, X ∧ Y,X∩Y, XY
- For X+Y allow X OR Y, X v Y, X U Y
- For $\overline{X}$ allow NOT X, ¬X

Or by truth table M = marking point

| | | | M | | | M | M | | M |
|---|---|---|---|---|---|---|---|---|---|
| A | B | A.B | $\overline{A.B}$ | $\overline{B}$ | $\overline{A.B}$ | $\overline{A.\overline{B}}$ | $\overline{A.B}$ + | $\overline{A.\overline{B}}$ | 1 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | | |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | | |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | | |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | | |



*Max 3 for stages, 1 for final answer* **4**

**[9]**

## Q10.

| G | H | K |
|---|---|---|
| 0 | 1 | 1 |
| 1 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 0 | 1 |
| ; | ; | ; |

*1 mark for each correct column*

**[3]**

## Q11.

(a)

| OR Gate | | |
|---|---|---|
| Input A | Input B | Output Q |
| 0 | 0 | **0** |
| 0 | 1 | **1** |
| 1 | 0 | **1** |
| 1 | 1 | **1** |

1 mark

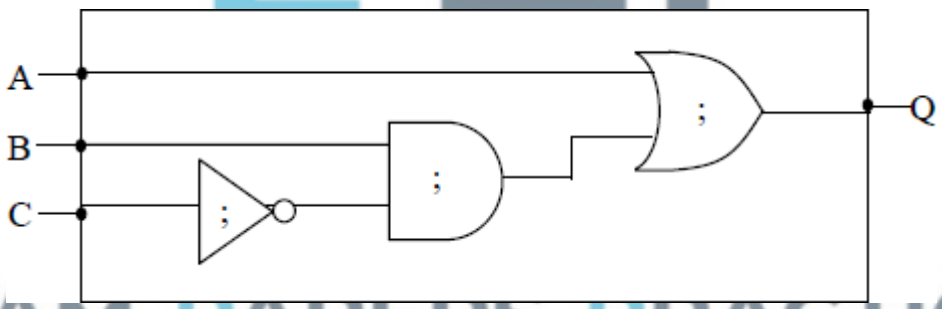
| XOR Gate | | |
|---|---|---|
| Input A | Input B | Output Q |
| 0 | 0 | **0** |
| 0 | 1 | **1** |
| 1 | 0 | **1** |
| 1 | 1 | **0** |

1 mark

*1 mark for each correct output column*
**A** True for 1, False for 0

2

(b)






*1 mark for NOT gate correctly linked to input C;*
*1 mark for AND gate correctly linked to B and* $\overline{C}$ *as input;*
**A** if AND gate linked directly to C
*1 mark for OR gate with inputs from A and the output of an AND gate and output connected to Q;*

3

(c) **Algebraic solution:**

B.( A + $\overline{B}$ )
*B.A + B.* $\overline{B}$ [*1 mark for expansion of brackets* ]
*B.A + 0* [*1 mark for identifying that B.*$\overline{B}$ *= 0* ]
*B.A* [*1 mark for correct answer*]

**Truth table solution:**

| | | X | Y | Z |
|---|---|---|---|---|
| A | B | $\overline{B}$ | $A+\overline{B}$ | $B\cdot(A+\overline{B})$ |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 |

*1 mark for both columns X and Y correct*
*1 mark for column Z correct*
*1 mark for correct answer (B.A)*

***Any other method:***
*If student has used any other method to arrive at correct answer then award marks as follows:*
*1 mark for correct answer, no working out*
*2 marks for correct answer with working out, not all steps shown.*
*3 marks for correct answer with all steps of working out shown.*

**A** True for 1, False for 0
**A** alternative notations :

- For X.Y allow X AND Y, X∧Y ,X∩Y, XY
- For X+Y allow X OR Y, X∨Y , XUY
- For $\overline{X}$ allow NOT X, ¬X

3

**[8]**

## Q12.

(a) 1; **A** True
1; **A** True
0; **A** False

3

(b) (i) AND and NOT

1

(ii) NAND // NAND gate
**R** NOT AND

1

(c) Minimise cost of production;
Reduce propagation delay//speed up processing;
Minimise heat generated;
Reduce power consumption;
**NE** simpler to produce/makes circuit simpler
**NE** reduce number of gates in chip

1

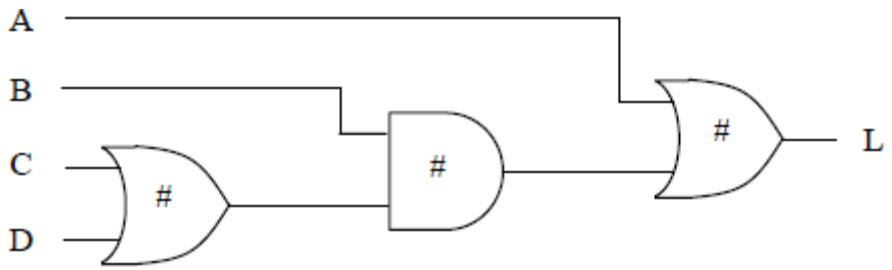
**[6]**

## Q13.

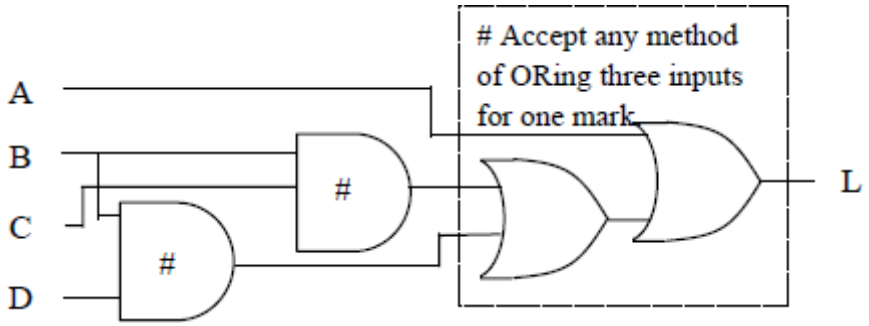
(a) NOR (Gate)
**I** case of answer i.e. nor is allowed

1

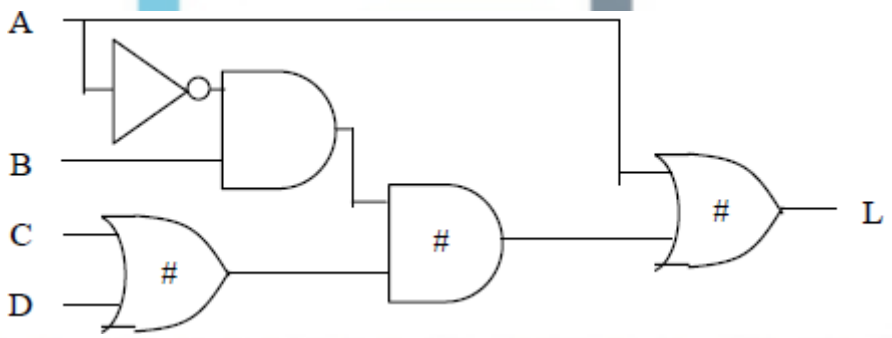
(b) (i) Solution 1:




Solution 2:

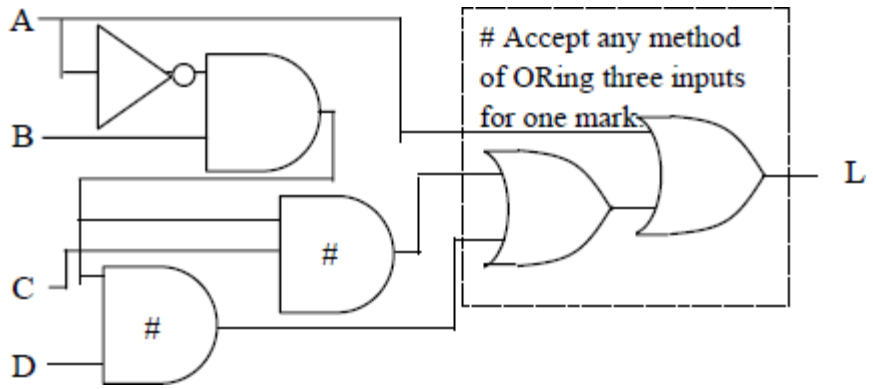



Solution 3 (solution 1 plus check for A off):






Solution 4 (solution 2 plus check for A off):




*1 mark for each correctly linked gate that is marked with a #*

**A** 3-input OR gate
**P1** for any unnecessary gates in a solution that would otherwise get 3 marks.
**P1** for any solution that would not correctly implement the logic but would otherwise get 3 marks.

*Mark from left to right until first mistake encountered then from right to left. When marking left to right award 1 mark for each gate correctly connected to its inputs. When marking right to left award 1 mark for each gate correctly connected to its output.*

**3**

(ii) A + B.(C+ D)
A + B.C+ B.D
A + $\overline{A}$.B. (C+ D)
A + $\overline{A}$.B.C+ $\overline{A}$.B.D

**A** Insertion of extra brackets that do not affect logic of expression
Note: Expression does not need to match diagram drawn in (i).
**A** alternative notations :

- For X.Y allow X AND Y, X ∧ Y , X ∩ Y, XY
- For X+Y allow X OR Y, X ∨ Y , X ∪ Y
- For $\overline{X}$ allow NOT X, ¬X

**1**

(c) **Algebraic Solution:**

$\overline{\overline{A} + \overline{B}}$ + B.$\overline{A}$ [Application of DeMorgan's Law *1 mark*]
A.B + B.$\overline{A}$ [Common term B taken out *1 mark*]
B.(A + $\overline{A}$) // B.1
B [Correct answer *1 mark*]

**A** alternative notations :

- For X.Y allow X AND Y, X ∧Y , X ∩ Y, XY
- For X+Y allow X OR Y, X∨ Y , X∪Y
- For X allow NOT X, ¬X

**Truth Table Solution:**

| | | | | X | Y | Z |
|---|---|---|---|---|---|---|
| A | B | $\overline{A}$ | $\overline{B}$ | $\overline{\overline{A}+\overline{B}}$ | $B \cdot \overline{A}$ | $\overline{\overline{A}+\overline{B}}+B \cdot \overline{A}$ |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 |

*1 mark for both columns X and Y correct*
*1 mark for column Z correct*
*1 mark for correct answer (B)*

**A** Rightmost column labelled as L or Q

**3**

**[8]**

## Q14.

(a)

**AND**

| Input A | Input B | Output |
|---|---|---|
| 0 | 0 | **0** |
| 0 | 1 | **1** |
| 1 | 0 | **1** |
| 1 | 1 | **1** |

**OR**

| Input A | Input B | Output |
|---|---|---|
| 0 | 0 | **0** |
| 0 | 1 | **0** |
| 1 | 0 | **0** |
| 1 | 1 | **1** |

*1 mark per correct table*

2

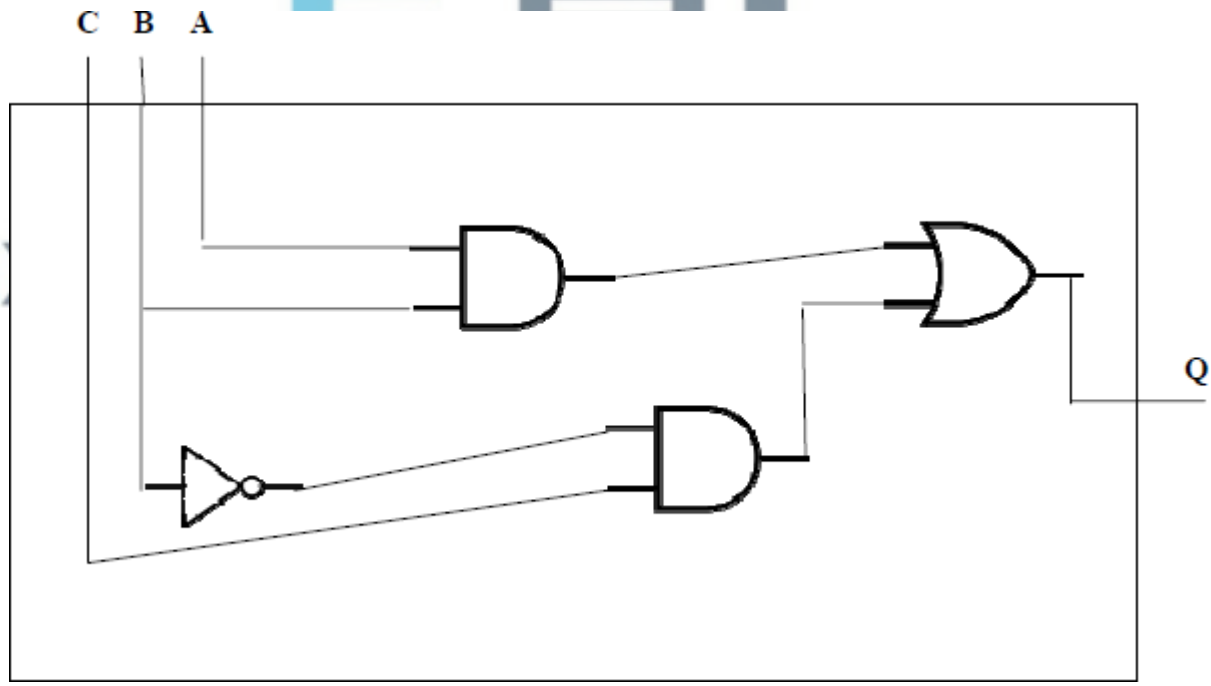
(b) (i) $Q = A.B + C.\overline{B}$

*1 mark for A.B or for $C.\overline{B}$*
*2 marks for $A.B + C.\overline{B}$*

**A** AND instead of .
**A** OR instead of +

2

(ii) *1 mark for each gate with correct inputs;;;;*
*Allow two lines from B*




4

**[8]**

Examiner reports

## Q1.

(a) This question part was well answered with just under three quarters of students fully completing the truth table for the logic circuit. The most common error made by those who did not was either failing to recognise the symbol for the XOR gate or not knowing the correct logic for this gate.

(b) Over two thirds of students achieved full marks for this question part by correctly writing a Boolean expression for the circuit. Common mistakes were to miss out brackets or add in brackets which affected the order of evaluation and made the expression incorrect or to use an incorrect symbol for XOR. Responses may be written using the words AND, OR, XOR etc if a student prefers this to using the Boolean algebra symbols.

(c) Just under half of the students recognised that the circuit was a full adder. A common incorrect response was that it was a flip-flop.

## Q3.

Students continue to be well prepared for questions based around logic gates and circuit drawing. The majority of students secured high marks for all question parts. When drawing circuits a few students swapped over the AND and OR symbols. It was also hard, occasionally, to spot any difference between the drawing of AND and OR symbols.

## Q4.

Overall, candidates continue to demonstrate a good understanding of logic and Boolean algebra.

(a) For this part candidates demonstrated a secure knowledge of the basic logic gates with around 75% achieving the two marks. A few candidates struggled with the NAND gate.



(b) The majority of candidates secured full marks for this part which asked for a logic circuit to be connected up. It was pleasing to see that candidates could identify the symbols for each logic gate and follow a relatively complex equation.

The simplification of a Boolean expression remains a challenging part of the paper with around a third of students not managing to secure any marks. Completing a logic table perhaps enabled weaker students to pick up some of the marks and should be a skill candidates can switch to if they find Boolean algebra too challenging. A third of candidates secured all of the marks and from their working it was clear that they could apply De Morgan's laws effectively and then factorise out a common element.

## Q5.

The majority of students performed well across this question but it was the Boolean simplification parts that caught out some students.

Part (a) had over half of all students gaining full marks for identifying the logic gates for each truth table correctly. The NOR gate proved to be the most challenging truth table to decipher. The three simplification parts appeared to get progressively harder for students working through the paper. It is to be noted again that students do appear to understand

that a law of De Morgan needs to be used but they apply it across the whole expression rather than carefully separating it into a left and right part with one operation in the middle.

Part (c) had over 80% of students securing full marks and was answered well. Mistakes came only from students placing the gates in the wrong order or drawing gates incorrectly.

## Q6.

A large number of students secured all 3 marks for drawing out the logic circuit required for part (a) and it was also pleasing to see the neatness of the majority of the diagrams. Mistakes identified included connecting pairs of not gates to each input.

The truth tables in part (b) were also answered well with the majority of students securing all of the marks.

Given that the students performed very well with the early parts of this question, it was perhaps surprising to see the number of students who did not secure any marks in part (d). On this paper, students were free to use any method to simplify the Boolean expression and those that tried a truth table method, in general, were able to pick up at least one mark. It is obvious that some of the weaker students just attempt a simple guess at the final answer because in previous papers it has been just A, for example. It also appeared that some students tried to tackle this question by applying De Morgan's in many different ways, not realising that there are other ways to go about simplifying.

## Q7.

Students are continuing to demonstrate that they can answer questions concerning logic gates and Boolean algebra. The majority could correctly fill in both of the truth tables for part (a).

Questions parts (b)(i) and (ii) had the majority of students securing 2 or 3 of the 3 marks available. Whilst it might be considered a harder skill to take some descriptive text and turn it into a logical statement, it was pleasing to see most students had a good attempt at this.



Part (c) appeared to be the most difficult section of this question and whilst students demonstrated that they might know De Morgan's law, they failed to apply it correctly. Sometimes this was obvious with a student writing out the laws next to their working. Students often switched both signs of the provided expression at once, rather than correctly separating it into two parts and therefore only changing one sign. Students who completed the De Morgan's part correctly then tended to go on and secure the other 2 marks.

## Q8.

On previous papers students have always done well in identifying logic gates but on this paper only around half correctly identified the XOR gate by writing a correct expression.

Over 90% of students correctly wrote the second expression and this highlights the case for further work on XOR gates. Based on the evidence seen in this and previous papers, students seem to be less familiar with XOR, NAND and NOR gates than OR, AND and NOT gates.

The truth table was completed well by the majority of students with only a small number of students not scoring any marks.

Identifying the arithmetic function was asked to probe students' understanding and it was

pleasing to see students supplying the correct answer of addition with some students recognising that the circuit was a half-adder.

Part (d) was asked in order to test the students' ability to simplify a Boolean expression using known identities. Students went down various routes to attempt to simplify the expression with expanding the brackets being the most common. It was pleasing to see a group of students solve by starting with the distributive identity and this usually meant that a full solution was found very quickly. It was common for weaker students just to remove completely the brackets and to then start working with the expression.

Very few students did not attempt to solve this question part using the required method. It is important to note that the specification states that students should, 'Be familiar with the use of De Morgan's laws and Boolean identities to manipulate and simplify simple Boolean expressions.' Truth tables can also be useful tools for simplification, but they only work well in quite specific circumstances and the specification requires that students are aware of how to simplify using Boolean identities.

## Q9.

Part (a) asked candidates to complete truth tables for a NAND and a NOR gate. It was pleasing to see that most candidates could secure both marks for this part. A few candidates answered the wrong way around whilst others provided the truth table for a XOR gate rather than a NOR gate.

The majority of candidates scored very well in part (b) securing full marks for the correct drawing of the logic circuit. The most common mistake was to put the AND gate before the NOT. Some candidates did not understand which gates related to each operator in the equation and therefore had the AND and OR gates swapped around.

Part (c) asked candidates to simplify a Boolean expression and a variety of methods were used. Candidates were awarded marks for a method where it was clear that a required skill was being used. When showing stages of working we would encourage candidates to make sure they only perform one step at a time. Good candidates also provided the rules they were using as explanation of their method. Candidates who realized that De Morgan's law could be applied to both sides of the equation and did this correctly quite quickly secured two marks for the method. A few candidates stopped when they reached a certain position not realizing that they could simplify further. The candidates who attempted this question using a truth table method tended to also score well.



## Q10.

This question asked candidates to complete a truth table for a logic circuit with multiple gates. Many candidates gave fully correct answers. A few candidates misidentified the NAND gate as an AND gate.

The majority of candidates secured the mark for G which was an OR gate. The combining of gates for the H and K answers caused problems for weaker candidates.

## Q11.

The question about Boolean logic, truth table and logic diagrams was answered much better than in previous years. This may be because the parts concerning drawing a logic diagram and simplifying a Boolean equation were a little more straightforward than those which had previously been asked. The truth table for an OR gate was completed more accurately than that for an EOR gate. The logic diagram often gained three marks and for the first time it was to see just three components drawn in the diagram rather than a whole series of symbols. The shapes of some of the symbols were far from ideal but those that

were nearly there were accepted rather than rejected. The hardest part of the question, simplifying Boolean expression, was also the one that gained least marks. It was however gratifying to see that on the whole it was answered far better than similar questions in previous years. Candidates often left out the intermediate step we required and this was where most marks were lost. There were still some candidates who made no attempt at this question.

## Q12.

The majority of candidates answered part (a) very well. It would seem that, given a logic gate diagram and a truth table made it quite easy for the candidates to answer when compared with Question 2 on Boolean algebra.

Part (b) was also well answered. The gates that could be replaced were usually correctly stated, however AND and NOR and NOT and OR sometimes appeared incorrectly. It was obvious from the answers that most candidates could convert the AND gate followed by a NOT gate into a NAND gate.

Part (c) was weakly answered even though there was a wide range of potential answers for a single mark. Where candidates went wrong was in giving answers about “making it easier for humans to understand and / or interpret”. Reducing the number of gates would reduce the propagation delay, thus speeding up processing. It could also reduce power consumption and the cost of manufacturing the circuit.

## Q13.

Some candidates correctly identified the truth table as representing the NOR logic gate, but there was a wide range of different responses to this question part.

The logic circuit question was well answered with many candidates getting two or three of the three available marks. Most realised that it was not necessary to NOT the A and AND it with B, although candidates were not penalised if they did this. Diagrams were usually drawn clearly.

Many candidates were able to state a correct Boolean expression that represented the logic circuit. Some introduced unnecessary brackets into the expression, but these were not penalised if they did not affect the expression’s logic.



Most candidates attempted to simplify the Boolean expression by applying the laws of Boolean algebra. A smaller number constructed a truth table which was also acceptable. When using the former method, many candidates recognised that the first step was to apply DeMorgan’s laws to the left hand part of the term, but fewer knew what to do after this step had been completed.

The most common mistake was to assume that A + B = A + B = A + B rather than applying De Morgan’s laws. Candidates need to ensure that they explicitly show all stages of their working out. A number of candidates scored a mark for having the correct final answer and for the application of De Morgan’s law, but lost a mark for not making the other steps in the simplification clear.

Candidates who produce truth table solutions to this type of question must ensure that they state the simplified expression at the end of their solution. A few produced an accurate truth table, but failed to state the resulting expression.

## Q14.

Most candidates had no difficulty completing the truth tables. It was pleasing to see that a large number of candidates correctly expressed the given scenario as a Boolean

equation. A few candidates mixed up the symbols for AND and OR. Many candidates correctly completed the logic gate diagram, even if they did not write down the correct Boolean expression. Each gate that had been given the correct inputs was awarded a mark. Some candidates drew very neat diagrams and helped themselves by writing the equation on the output of each gate. A few candidates missed out on marks because they had not connected the gates to each other.